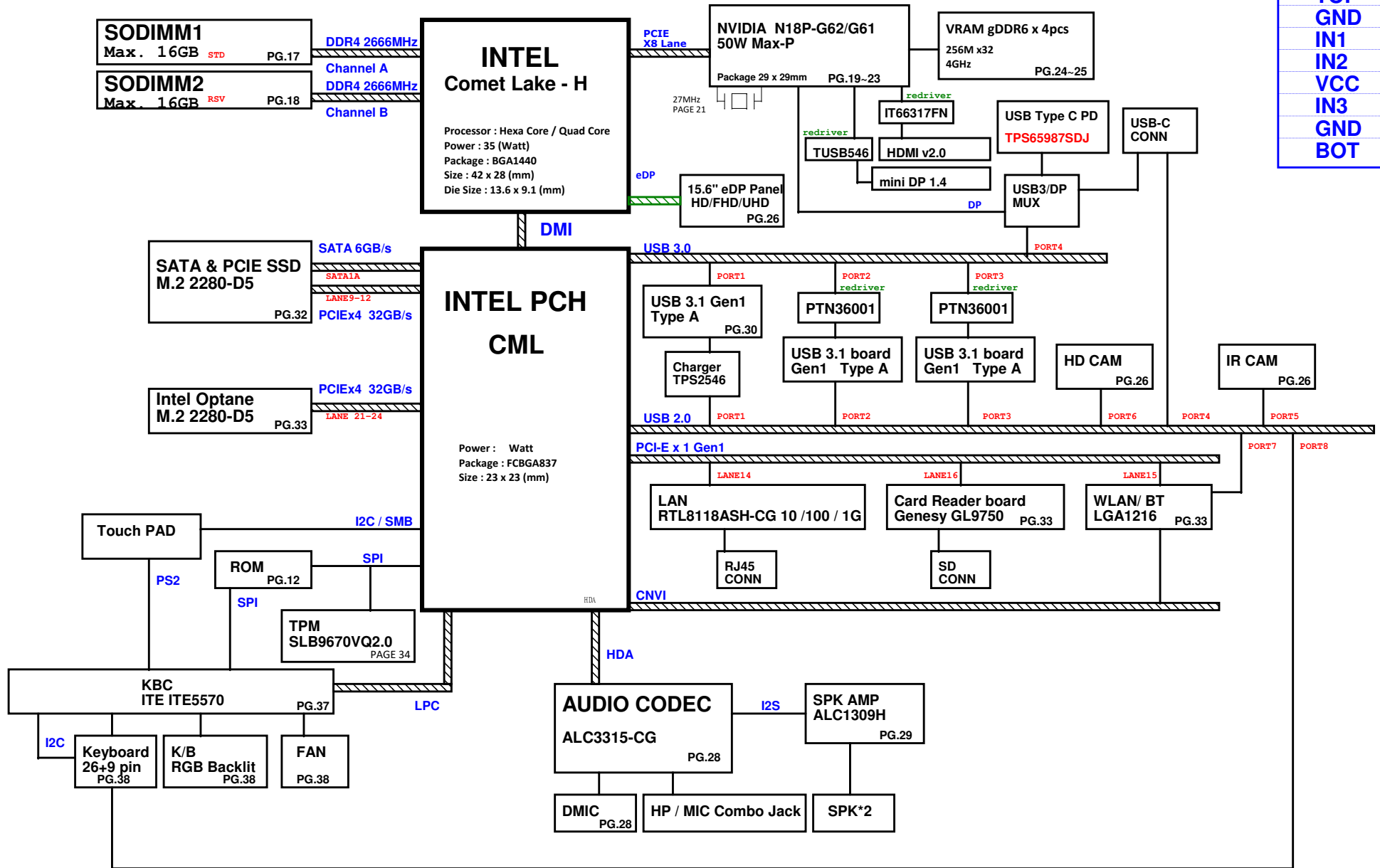


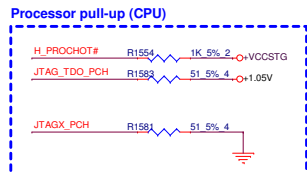
INTEL Comet Lake - H SYSTEM DIAGRAM

STACKUP

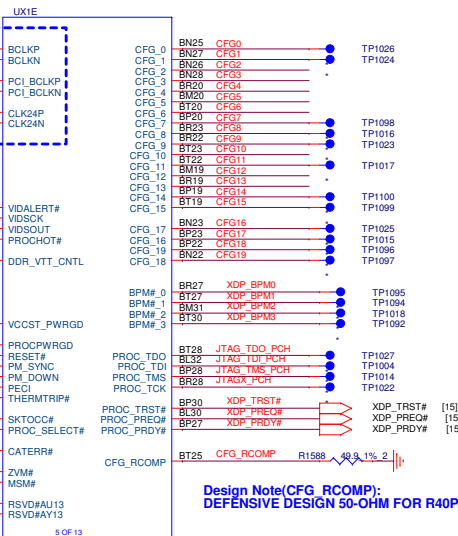
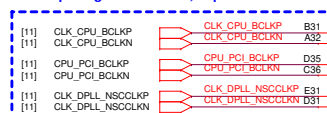
TOP
GND
IN1
IN2
VCC
IN3
GND
BOT



CML-H Processor (CLK, MISC, JTAG)



Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impedence 85 ohm

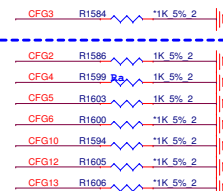


	CFG[4]	Ra
EDP Output from DGPU	Hi	Non Stuff
EDP Output from iGPU	Low	Stuff

Processor Strapping Switchable or Optimus CFG4 need stuff

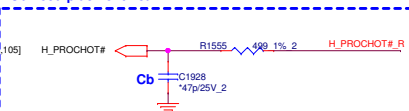
The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG
1, Disable;



Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placment near VR



Layout Notes:

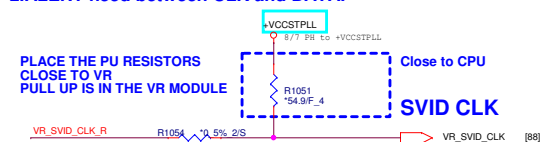
H_PWRGD (50ohm)
Trace Length: 1~11 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

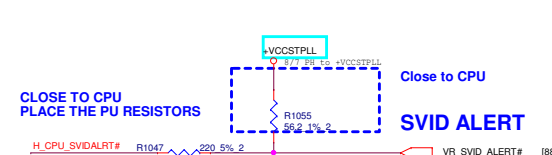
PM_SYNC (50ohm)
Trace Length: 1~11.25 inches

CPU CORE SVID

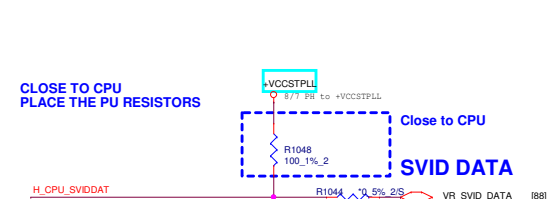
- Layout note:
1. Need routing together
 2. ALERT need between CLK and DATA.



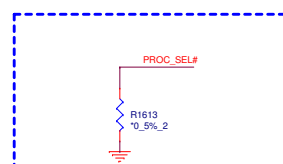
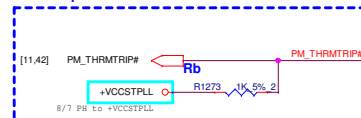
VR_SVID_CLK_R R1054 *0.5%



H_CPU_SVIDALRT# R1047 2

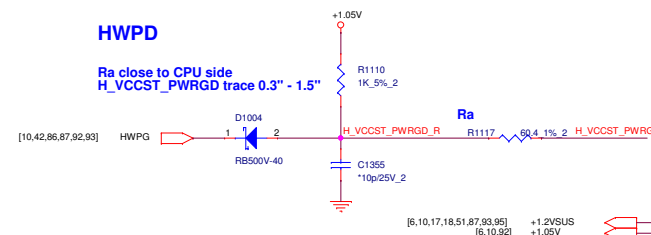


THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
Rb need placment near PCH



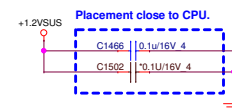
HWPD

Ra close to CPU side
H VCCST PWRGD trace 0.3" - 1.5"



CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A



CFL-H Processor (DMI, PEG, FDI)

+1.2VSUS [2,6,10,17,18,51,87,93,95]
+3VSS [10,12,14,23,31,35,38,42,47,48,51,82,86,88,92,93,95,104,105]
+3V [8,10,11,13,16,17,18,21,28,30,31,33,34,36,38,39,41,42,48,50,51,52,82,88,91,95,98,99,101,105]

Layout Note: PEG_RCOMP

Max Trace length = 600 MILS
Min Trace width = 5 MILS
Trace spacing to others = 15 MILS

dGPU

dGPU

DMI

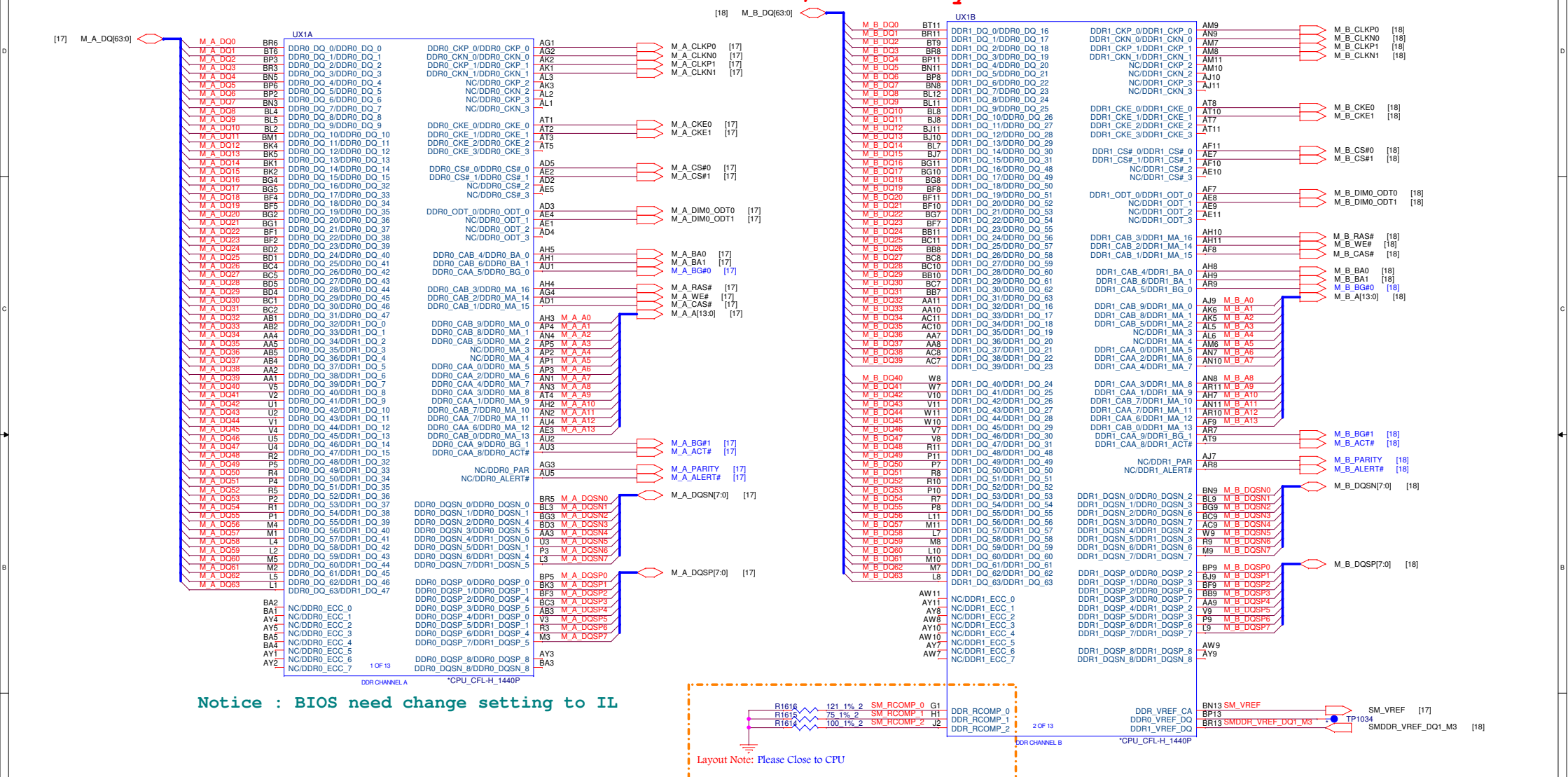
DMI

eDP



PROJECT : G3BE
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CFL-H Processor (DDR4)



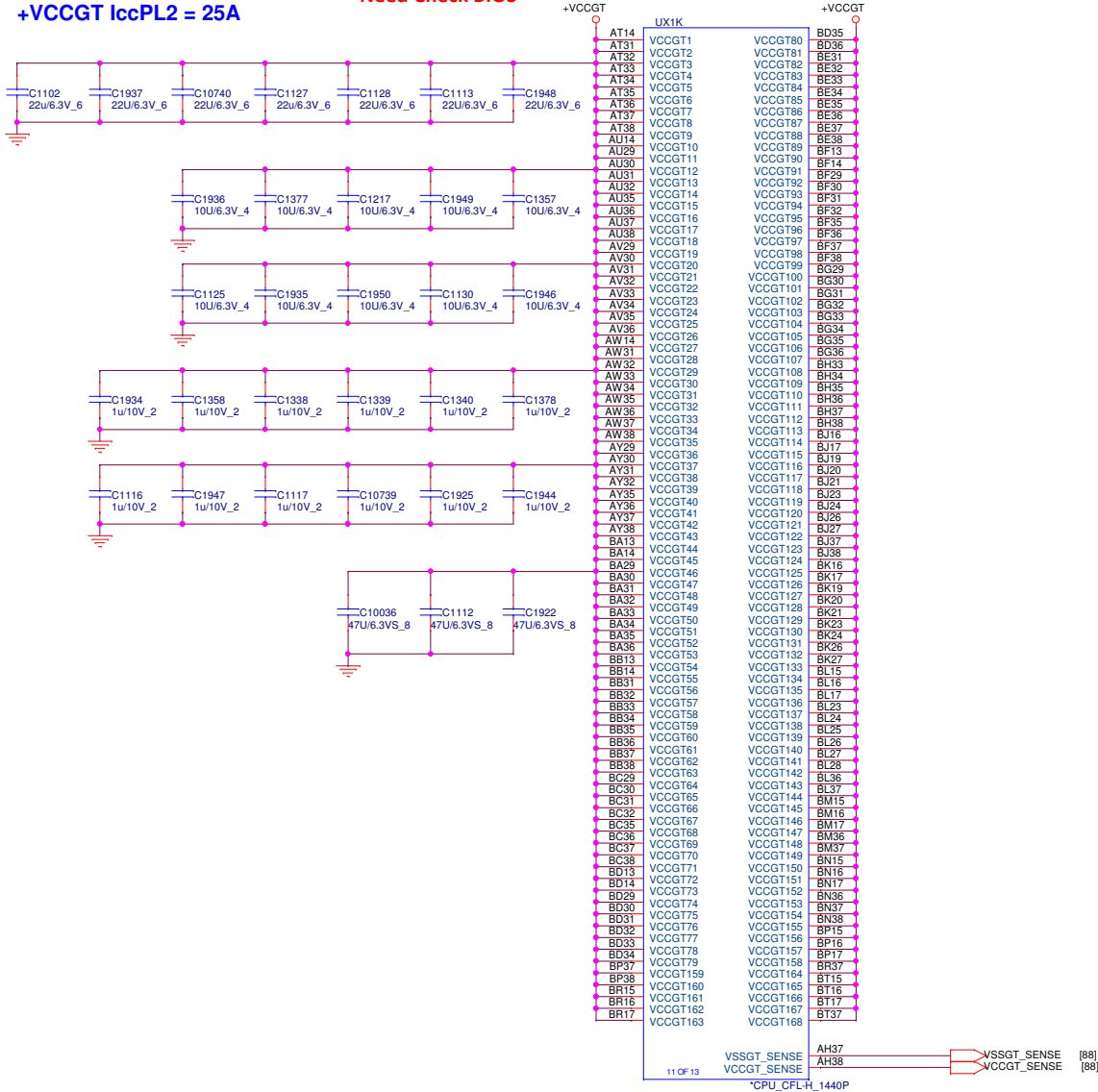
Notice : BIOS need change setting to IL

Layout Note: Please Close to CPU

SKYLAKE Processor (POWER)

From CFL-H Power Map
+VCCGT Iccmax = 32A
+VCCGT IccPL2 = 25A

Need Check BIOS

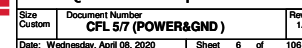


+VCCGT [88,91]
+1.2VSUS [2,6,10,17,18,51,87,93,95]

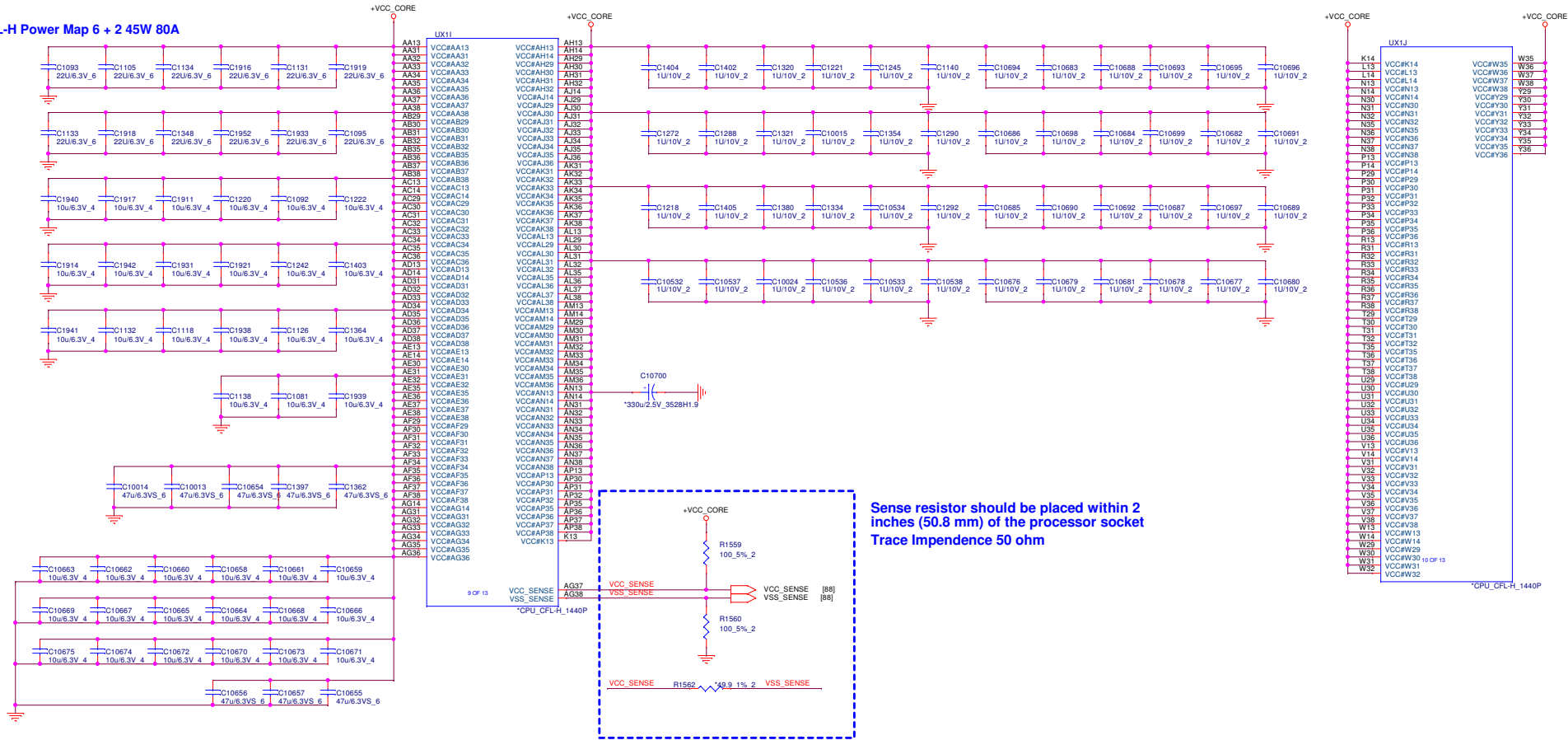


PROJECT : G3BE
Quanta Computer Inc.

Size Custom Document Number
CFL 4/7 (POWER)
Date: Wednesday, April 08, 2020 Sheet 5 of 106



Follow CFL-H Power Map 6 + 2 45W 80A



UX1F		
A10	VSS_1	VSS_82
A12	VSS_2	VSS_83
A16	VSS_3	VSS_84
A18	VSS_4	VSS_85
A20	VSS_5	VSS_86
A22	VSS_6	VSS_87
A24	VSS_7	VSS_88
A26	VSS_8	VSS_89
A28	VSS_9	VSS_90
A30	VSS_10	VSS_91
A6	VSS_11	VSS_92
A9	VSS_12	VSS_93
AA12	VSS_13	VSS_94
AA29	VSS_14	VSS_95
AA30	VSS_15	VSS_96
AB33	VSS_16	VSS_97
AB34	VSS_17	VSS_98
AB6	VSS_18	VSS_99
AC1	VSS_19	VSS_100
AC12	VSS_20	VSS_101
AC2	VSS_21	VSS_102
AC3	VSS_22	VSS_103
AC37	VSS_23	VSS_104
AC38	VSS_24	VSS_105
AC4	VSS_25	VSS_106
AC5	VSS_26	VSS_107
AC6	VSS_27	VSS_108
AD10	VSS_28	VSS_109
AD11	VSS_29	VSS_110
AD12	VSS_30	VSS_111
AD28	VSS_31	VSS_112
AD30	VSS_32	VSS_113
AD6	VSS_33	VSS_114
AD8	VSS_34	VSS_115
AD9	VSS_35	VSS_116
AE33	VSS_36	VSS_117
AE34	VSS_37	VSS_118
AE6	VSS_38	VSS_119
AF1	VSS_39	VSS_120
AF12	VSS_40	VSS_121
AF13	VSS_41	VSS_122
AF14	VSS_42	VSS_123
AF2	VSS_43	VSS_124
AF3	VSS_44	VSS_125
AF4	VSS_45	VSS_126
AG10	VSS_46	VSS_127
AG11	VSS_47	VSS_128
AG13	VSS_48	VSS_129
AG29	VSS_49	VSS_130
AG30	VSS_50	VSS_131
AG6	VSS_51	VSS_132
AG7	VSS_52	VSS_133
AG8	VSS_53	VSS_134
AH12	VSS_54	VSS_135
AH33	VSS_55	VSS_136
AH34	VSS_56	VSS_137
AH35	VSS_57	VSS_138
AH36	VSS_58	VSS_139
AH6	VSS_59	VSS_140
AJ1	VSS_60	VSS_141
AJ13	VSS_61	VSS_142
AJ2	VSS_62	VSS_143
AJ3	VSS_63	VSS_144
AJ37	VSS_64	VSS_145
AJ38	VSS_65	VSS_146
AJ4	VSS_66	VSS_147
AJ5	VSS_67	VSS_148
AJ6	VSS_68	VSS_149
W4	VSS_69	VSS_150
W5	VSS_70	VSS_151
Y10	VSS_71	VSS_152
Y11	VSS_72	VSS_153
Y13	VSS_73	VSS_154
Y14	VSS_74	VSS_155
Y37	VSS_75	VSS_156
Y38	VSS_76	VSS_157
Y7	VSS_77	VSS_158
Y8	VSS_78	VSS_159
Y9	VSS_79	VSS_160
AK29	VSS_80	VSS_161
AK30	VSS_81	VSS_162

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*CPU_CFL-H_1440P

UX1G		
AW5	VSS_163	VSS_244
AY12	VSS_164	VSS_245
AY33	VSS_165	VSS_246
AY34	VSS_166	VSS_247
B9	VSS_167	VSS_248
BA10	VSS_168	VSS_249
BA11	VSS_169	VSS_250
BA12	VSS_170	VSS_251
BA37	VSS_171	VSS_252
BA39	VSS_172	VSS_253
BA6	VSS_173	VSS_254
BA7	VSS_174	VSS_255
BA8	VSS_175	VSS_256
BA9	VSS_176	VSS_257
BB1	VSS_177	VSS_258
BB12	VSS_178	VSS_259
BB2	VSS_179	VSS_260
BB29	VSS_180	VSS_261
BB3	VSS_181	VSS_262
BB30	VSS_182	VSS_263
BB4	VSS_183	VSS_264
BB5	VSS_184	VSS_265
BB6	VSS_185	VSS_266
BC12	VSS_186	VSS_267
BC13	VSS_187	VSS_268
BC14	VSS_188	VSS_269
BC33	VSS_189	VSS_270
BC34	VSS_190	VSS_271
BC6	VSS_191	VSS_272
BD10	VSS_192	VSS_273
BD11	VSS_193	VSS_274
BD12	VSS_194	VSS_275
BD37	VSS_195	VSS_276
BD6	VSS_196	VSS_277
BD7	VSS_197	VSS_278
BD9	VSS_198	VSS_279
BD9	VSS_199	VSS_280
BE1	VSS_200	VSS_281
BE2	VSS_201	VSS_282
BE29	VSS_202	VSS_283
BE3	VSS_203	VSS_284
BE30	VSS_204	VSS_285
BE4	VSS_205	VSS_286
BE5	VSS_206	VSS_287
BE6	VSS_207	VSS_288
BF12	VSS_208	VSS_289
BF33	VSS_209	VSS_290
BF34	VSS_210	VSS_291
BF6	VSS_211	VSS_292
BG12	VSS_212	VSS_293
BG13	VSS_213	VSS_294
BG14	VSS_214	VSS_295
BG37	VSS_215	VSS_296
BG38	VSS_216	VSS_297
BG6	VSS_217	VSS_298
BH1	VSS_218	VSS_299
BH10	VSS_219	VSS_300
BH11	VSS_220	VSS_301
BH12	VSS_221	VSS_302
BH14	VSS_222	VSS_303
BH2	VSS_223	VSS_304
BH3	VSS_224	VSS_305
BH4	VSS_225	VSS_306
BH5	VSS_226	VSS_307
BH6	VSS_227	VSS_308
BH7	VSS_228	VSS_309
BH8	VSS_229	VSS_310
BH9	VSS_230	VSS_311
T2	VSS_231	VSS_312
T3	VSS_232	VSS_313
T33	VSS_233	VSS_314
T4	VSS_234	VSS_315
A14	VSS_235	VSS_316
T5	VSS_236	VSS_317
T6	VSS_237	VSS_318
T7	VSS_238	VSS_319
U37	VSS_239	VSS_320
W2	VSS_240	VSS_321
W3	VSS_241	VSS_322
W33	VSS_242	VSS_323
W34	VSS_243	VSS_324

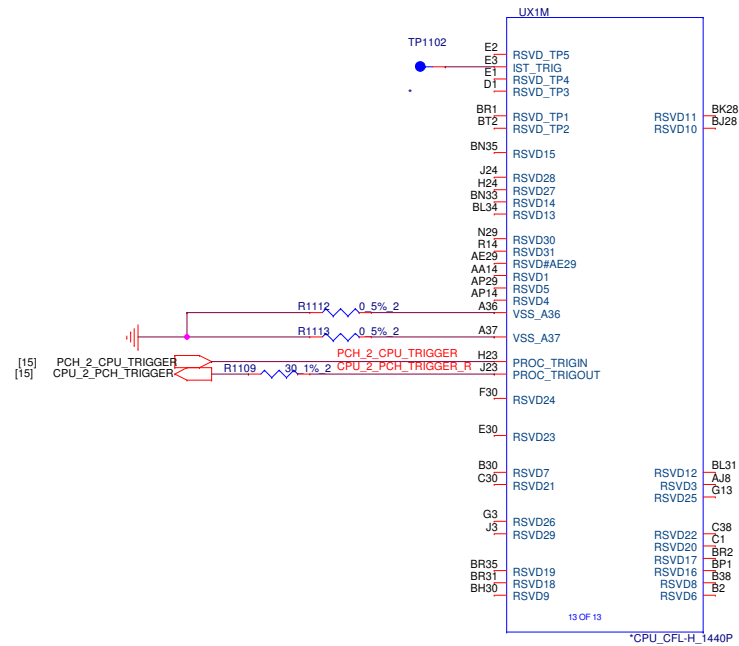
7 OF 13

*CPU_CFL-H_1440P

UX1H		
BN4	VSS_325	VSS_409
BN7	VSS_326	VSS_410
BP12	VSS_327	VSS_411
BP14	VSS_328	VSS_412
BP18	VSS_329	VSS_413
BP21	VSS_330	VSS_414
BP24	VSS_331	VSS_415
BP25	VSS_332	VSS_416
BP26	VSS_333	VSS_417
BP29	VSS_334	VSS_418
BP33	VSS_335	VSS_419
BP34	VSS_336	VSS_420
BP7	VSS_337	VSS_421
BR12	VSS_338	VSS_422
BR14	VSS_339	VSS_423
BR18	VSS_340	VSS_424
BR21	VSS_341	VSS_425
BR24	VSS_342	VSS_426
BR25	VSS_343	VSS_427
BR26	VSS_344	VSS_428
BR29	VSS_345	VSS_429
BR34	VSS_346	VSS_430
BR36	VSS_347	VSS_431
BR7	VSS_348	VSS_432
BT12	VSS_349	VSS_433
BT14	VSS_350	VSS_434
BT18	VSS_351	VSS_435
BT21	VSS_352	VSS_436
BT24	VSS_353	VSS_437
BT26	VSS_354	VSS_438
BT29	VSS_355	VSS_439
BT32	VSS_356	VSS_440
BT5	VSS_357	VSS_441
C11	VSS_358	VSS_442
C13	VSS_359	VSS_443
C15	VSS_360	VSS_444
C17	VSS_361	VSS_445
C19	VSS_362	VSS_446
C21	VSS_363	VSS_447
C23	VSS_364	VSS_448
C25	VSS_365	VSS_449
C27	VSS_366	VSS_450
C29	VSS_367	VSS_451
C31	VSS_368	VSS_452
C37	VSS_369	VSS_453
C5	VSS_370	VSS_454
C8	VSS_371	VSS_455
C9	VSS_372	VSS_456
D10	VSS_373	VSS_457
D12	VSS_374	VSS_458
D14	VSS_375	VSS_459
D16	VSS_376	VSS_460
D18	VSS_377	VSS_461
D20	VSS_378	VSS_462
D22	VSS_379	VSS_463
D24	VSS_380	VSS_464
D26	VSS_381	VSS_465
D28	VSS_382	VSS_466
D3	VSS_383	VSS_467
D30	VSS_384	VSS_468
D33	VSS_385	VSS_469
D6	VSS_386	VSS_470
D9	VSS_387	VSS_471
E34	VSS_388	VSS_472
E35	VSS_389	VSS_473
E38	VSS_390	VSS_474
E4	VSS_391	VSS_475
E9	VSS_392	VSS_476
N3	VSS_393	VSS_477
N33	VSS_394	VSS_478
N34	VSS_395	VSS_479
N4	VSS_396	VSS_480
N5	VSS_397	VSS_481
N6	VSS_398	VSS_482
N7	VSS_399	VSS_483
N8	VSS_400	VSS_484
N9	VSS_401	VSS_485
P12	VSS_402	VSS_486
P38	VSS_403	VSS_487
M14	VSS_404	VSS_488
M6	VSS_405	VSS_489
N1	VSS_406	VSS_490
F11	VSS_407	VSS_491
F13	VSS_408	VSS_492

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*CPU_CFL-H_1440P



USB 2.0 PORT	
PORT1	USB2 MB
PORT2	USB2 DB-1
PORT3	USB2 DB-2
PORT4	USB2.0 For Type C
PORT5	NC
PORT6	CAMERA
PORT7	WLAN
PORT8	KB MCU
PORT9-14	NC

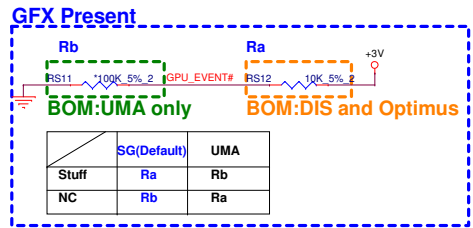
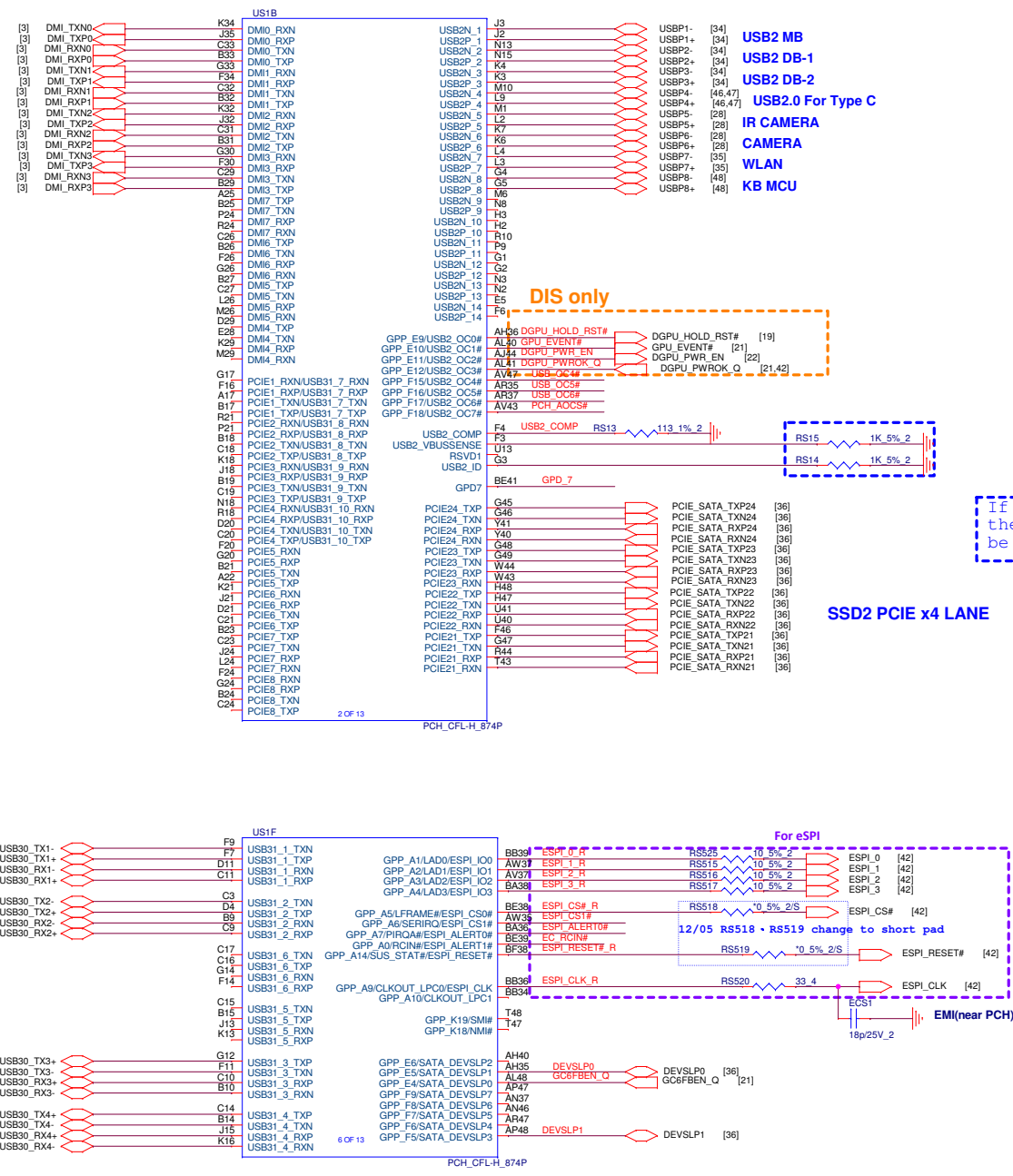
USB 3.0 PORT	
PORT1	USB3 MB AOU
PORT2	USB3.0 DB1
PORT3	USB3.0 DB2

USB3.0 (M/B)

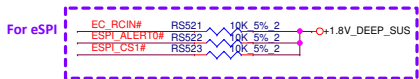
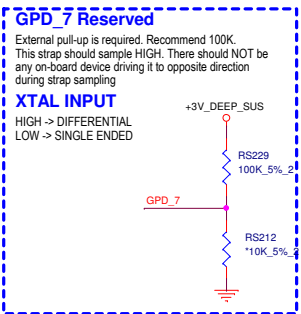
USB3.0 DB1

USB3.0 DB2

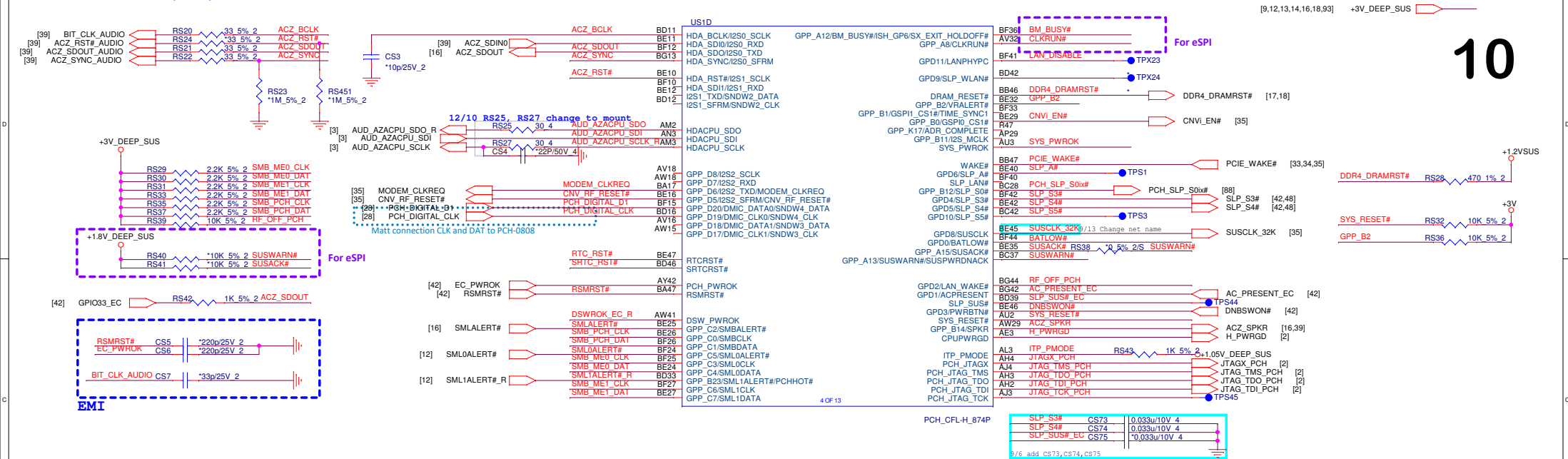
USB3.0 (Type C)



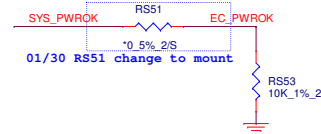
If OTG is not implemented on the platform, then USB2_ID and USB2_VBUSSENSE should both be connected to ground.



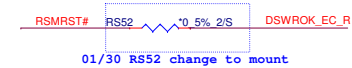
HDA Bus(CLG)



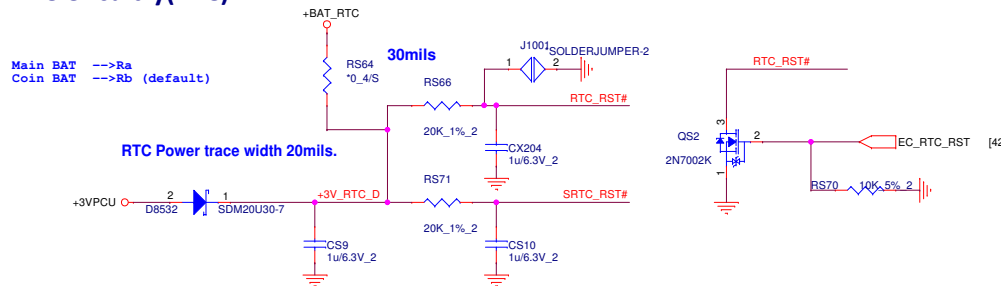
System PWR_OK(CLG)



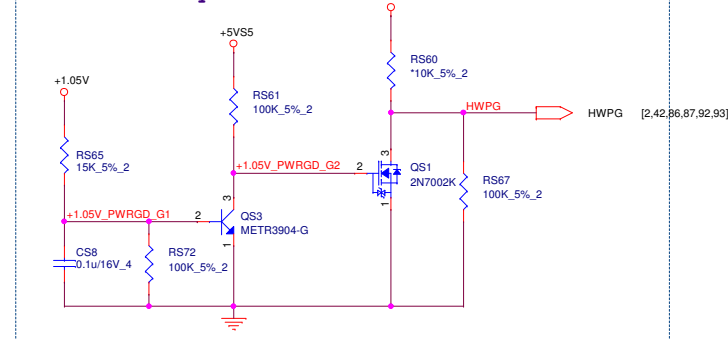
For DS3 Sequence



RTC Circuitry(RTC)



For HWPG Sequence



For Power Sequence.



For Power Sequence, pull high reuest



11

SSD PCIE x4 (SATA0A) LANE

SSD PCIE x4 LANE

WLAN

CardReader

Thunderbolt (NA)

NUMPAD ID:
without Numpad => High
with Numpad => Low

BOM:SSD only
For SSD Det (SATA0A)

GPIOS35/36:
SSD SATA IF => High
SSD PCIE IF => Low

PM_THRMTRIP#_P 0.3-2 inches

H_PECT (50ohm)
Trace Length: <0.5 inches
Ra,Ca need placement close to PCH.

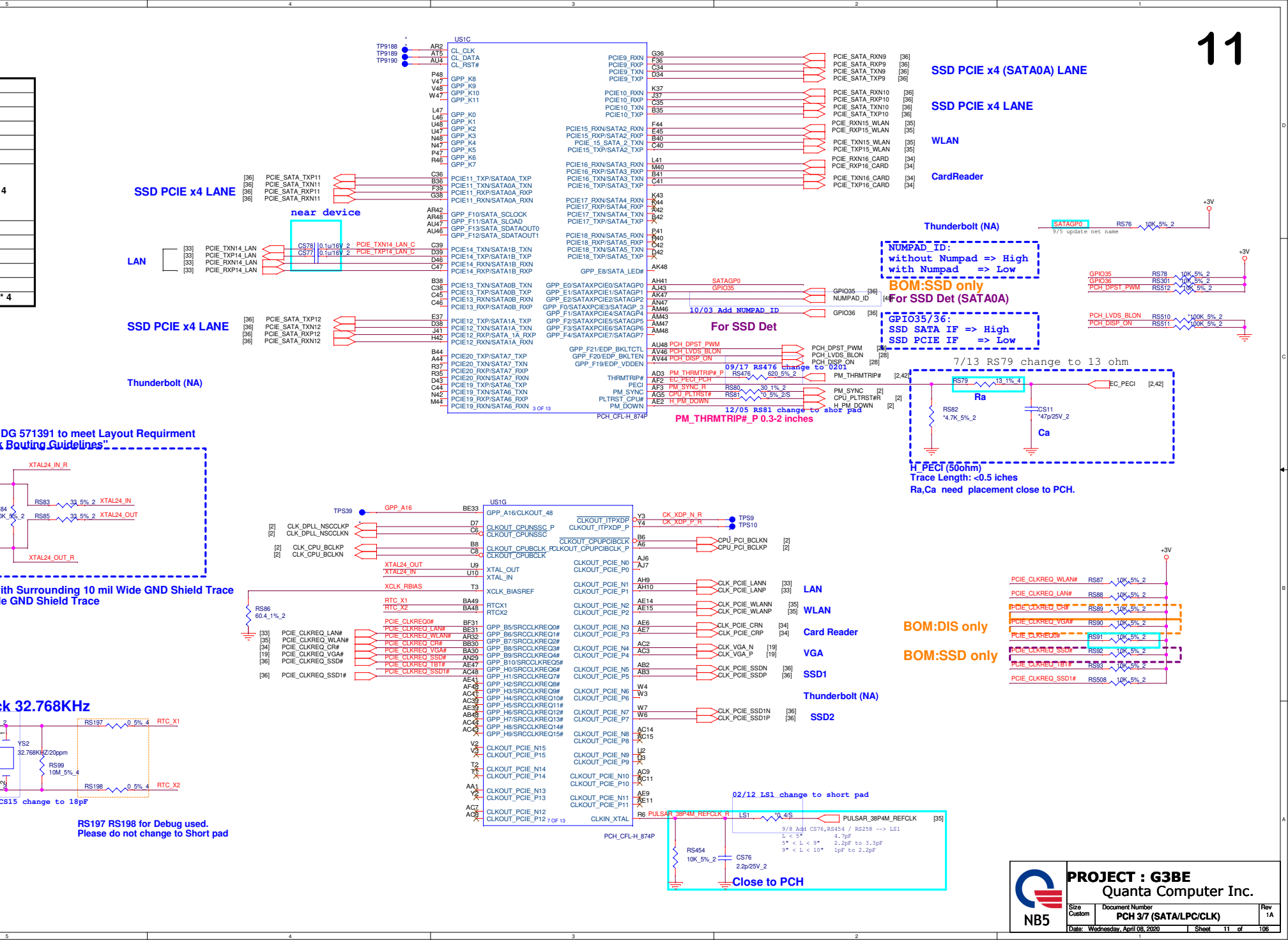
BOM:DIS only

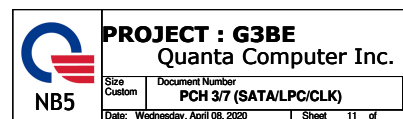
BOM:SSD only

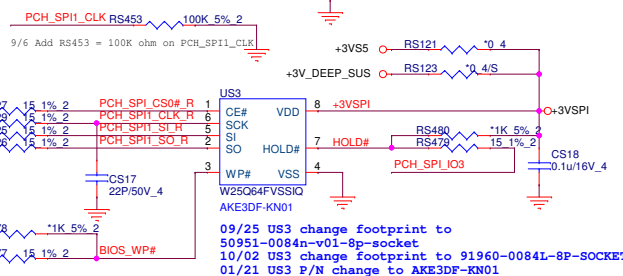
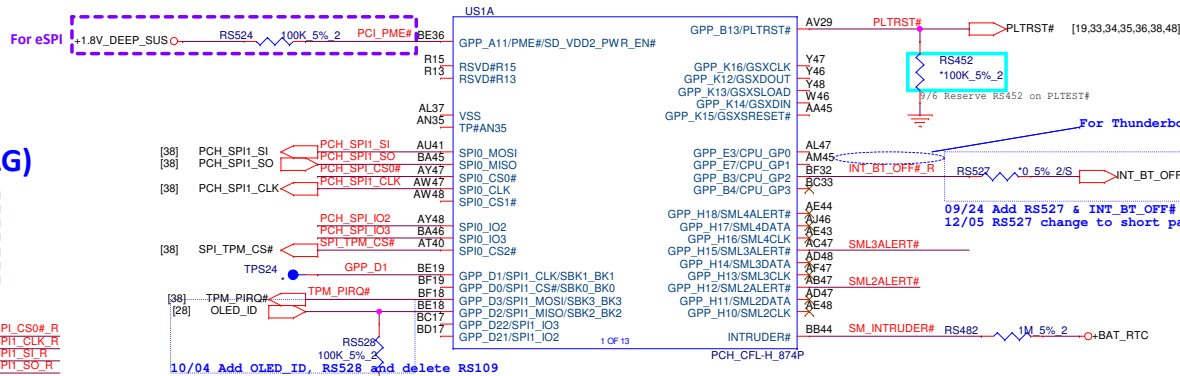
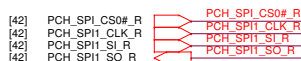
Close to PCH

PROJECT : G3BE
Quanta Computer Inc.

Size Custom
Document Number
PCH 3/7 (SATA/LPC/CLK)
Date: Wednesday, April 08, 2020
Sheet 11 of 106







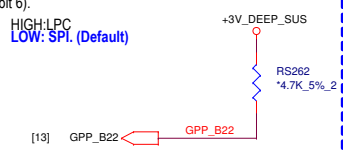
Pin Straps (Sheet 2 of 4)

Signal	Usage	When Sampled	Comment						
			<p>This Signal has a weak internal pull-down.</p> <p>This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (BusID, Device3, Function), offset DCH, bit 6).</p> <table><tr><th>Bit 6</th><th>Boot BIOS Destination</th></tr><tr><td>0</td><td>SPI (Default)</td></tr><tr><td>1</td><td>LPC</td></tr></table> <p>Notes:</p> <ol style="list-style-type: none">1. The internal pull-down is disabled after PCH_PFWROK is high.2. If option 1, LPC is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN.4. This signal is in the primary well.	Bit 6	Boot BIOS Destination	0	SPI (Default)	1	LPC
Bit 6	Boot BIOS Destination								
0	SPI (Default)								
1	LPC								
GPP_B22 / GSP11_MOST	Boot BIOS Strap bit BBS	Rising edge of PCH_PFWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = LPC is selected (for EC). 1 = eSPI is selected (for EC).</p> <p>Notes:</p> <ol style="list-style-type: none">1. The internal pull-down is disabled after RSMRST#2. This signal is in the primary well.						
GPP_CS / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	<p>Warning: If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' as well (SAFS is disabled)</p> <p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>						
SPIO_MOST	Reserved	Rising edge of RSMRST#	<p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>						
GPP_H15 / SML3ALERT#	Reserved	Rising edge of RSMRST#	<p>This signal has an internal pull-down.</p> <p>0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB</p> <p>Notes:</p> <ol style="list-style-type: none">1. The internal pull-down is disabled after RSMRST# de-asserts.2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. <p>This signal is in the primary well.</p>						
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	<p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>						
SPIO_102	Reserved	Rising edge of RSMRST#	<p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>						

BOOT SELECT STRAP

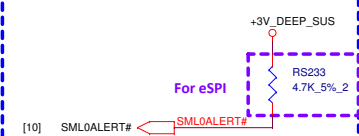
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6).

HIGH: LPC
LOW: SPI. (Default)



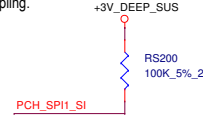
ESPI/LPC SELECT STRAP

- **HIGH:**eSPI Is selected for EC. (Default)
- **LOW:** LPC Is selected for EC.



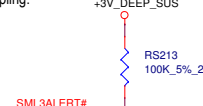
RESERVED

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



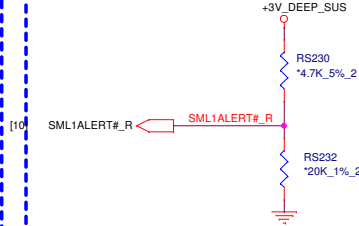
RESERVED

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



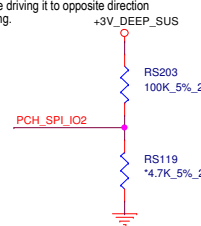
RESERVED

- This signal has an internal pull-down.
- 0 = Disable Intel® DCI-OOB (Default)
- 1 = Enable Intel® DCI-OOB



RESERVED

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

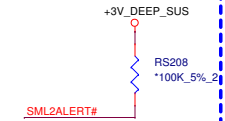


ESPI FLASH SHARING MODE

This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.

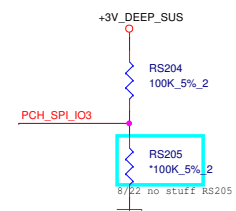
Notes:

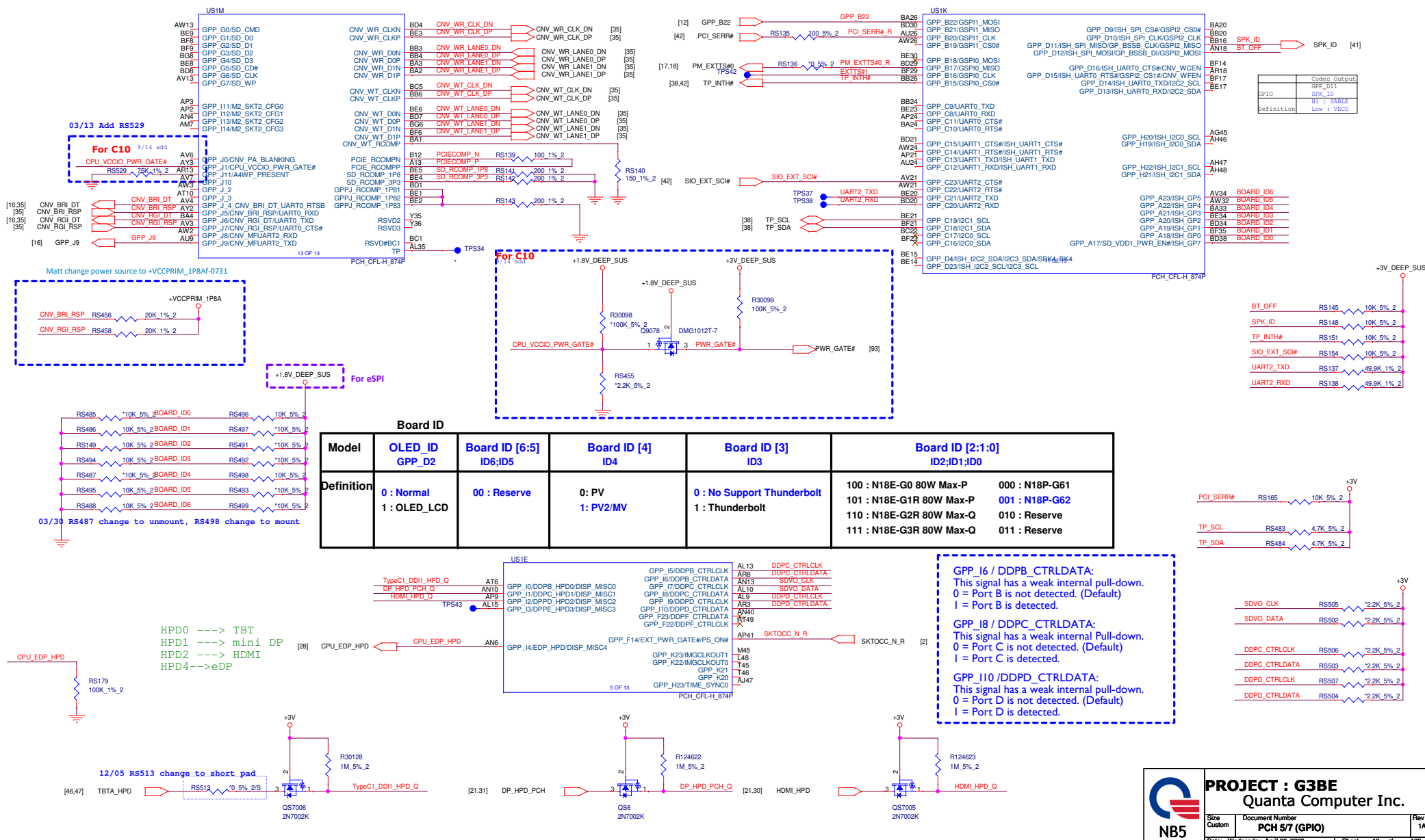
1. The internal pull-down is disabled after RSMRST de-asserts.
2. This signal is in the primary well.

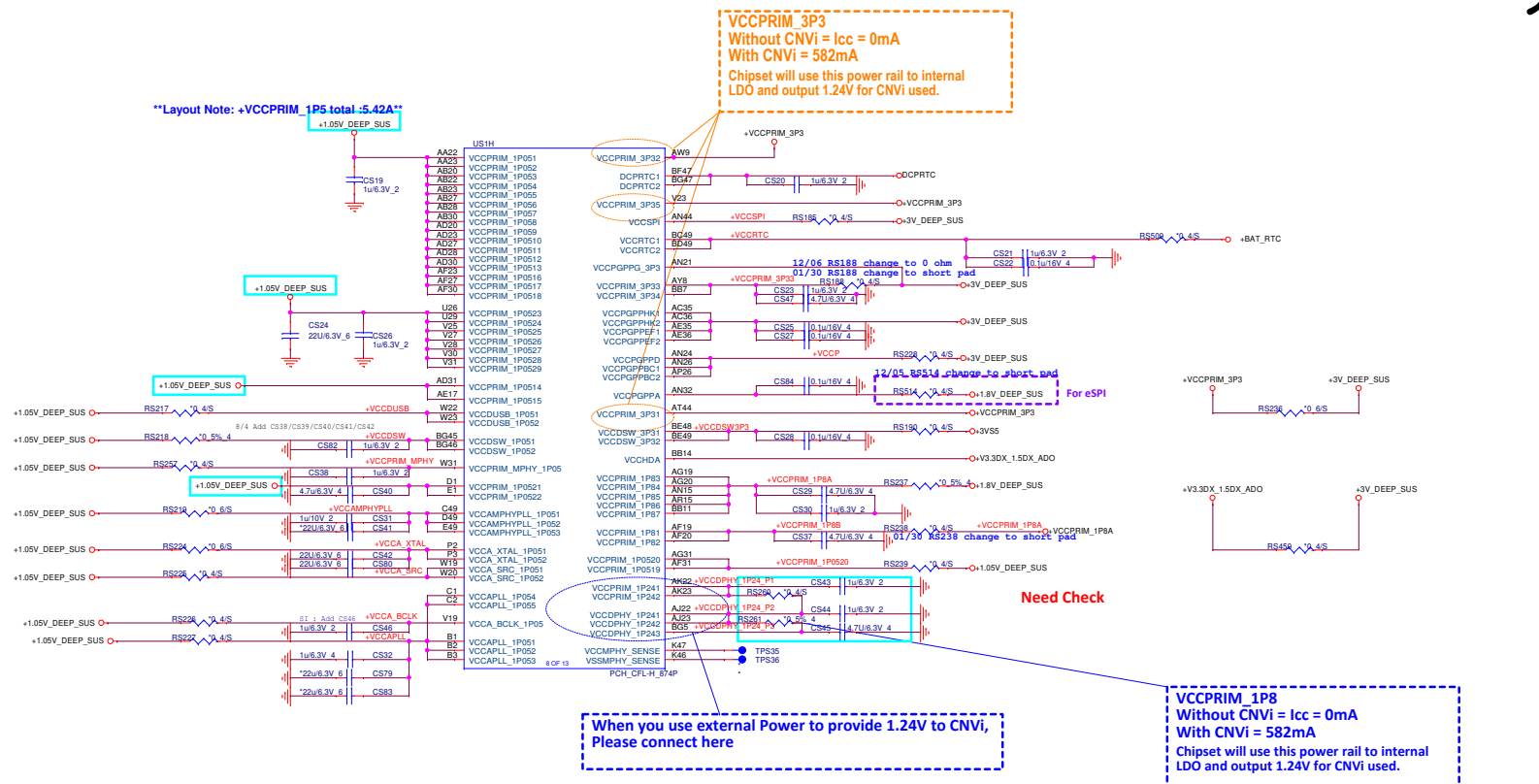


RESERVED

- External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
- This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.







Please follow below table to check Layout

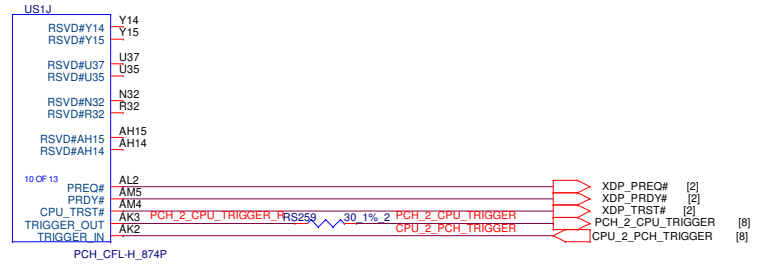
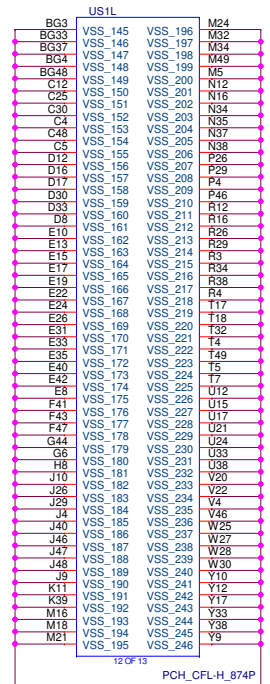
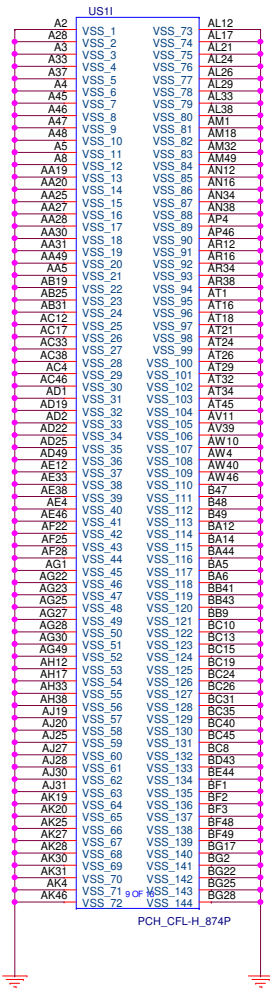
Table 10-4. PCH-H Estimated I_{cc}³ with Integrated 1.8V VRM Mode OFF (H Mobile SKUs)

Voltage Rail	Voltage (V)	S0 I _{cc} max Current ¹ (A)	Sx I _{cc} Idle Current ² (mA)	S0ix I _{cc} max Current (mA)	Deep Sx I _{cc} Idle Current (mA)	G3 (μA)
VCCAPLL_1P05	1.05	0.034	0.2	0.801	0	0
VCCA_BCLK_1P05	1.05	0.007	0.1	0.087	0	0
VCCA_SRC_1P05	1.05	0.141	0.3	0.838	0	0
VCCA_XTAL_1P05	1.05	0.005	0.544	0.195	0	0
VCCAMPHYPLL_1P05	1.05	0.114	0.4	1.192	0	0
VCCPRIM_1P05	1.05	4.174 HSD Lane Adder refer to Table 10-7 column HALO	40.344	0.477A	0	0
VCCPRIM_MPHY_1P0	1.05	0.088	0.2	1.22	0	0
VCCDSW_1P05	1.05	0.01	0.2	0.001	0.2	0
VCCDUSB_1P05	1.05	0.33	1.388	16.373	0	0
VCHDA	3.3	0.007	0.1	4.908	0	0
VCCDSW_3P3	3.3	0.094	0.2	0.705	1.05	0
VCCPRIM_3P3	3.3	0.318	0.3	0.916	0	0
VCCGPPA	3.3	0.085	0.1	0.103	0	0
VCCGPPBC	3.3	0.286	0.2	0.232	0	0
VCCGPPD	3.3	0.117	0.1	0.109	0	0
VCCGPPF	3.3	0.145	0.2	0.094	0	0
VCCGPPG_3P3	3.3	0.121	0.1	0.072	0	0
VCCGPPH	3.3	0.219	0.2	0.138	0	0
VCCPRIM_1P8	1.8	0.152 CNVi Adder refer to Table 10-4, column HALO	6.607	9.411	0	0
VCCRTC ¹	3.0	0.31mA	0.299	0.075	0.316	6
VCCSPI	3.3	0.042	0.1	0.153	0	0

Notes:

- The VCC rail ICC data is taken at 3.0V while the system is in a mechanical off (G3) state at room temperature.
- I_{cc}max estimates assumes 110 °C.
- The I_{cc}max value is a steady state current that can happen after respective power ok has asserted (or reset signal has de-asserted).
- Sx I_{cc} Idle assumes PCH is idle and ME is power gated.
- Sx I_{cc} at 3.3V level is assumed. Sx I_{cc} data at the 1.8 V and/or 1.5V level not measured.

[9,10,12,13,16,18,90] +3V_DEEP_SUS



Pin Straps (Sheet 1 of 4)

Signal	Usage	When Sampled	Comment
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = Disable "Top Swap" mode. (Default)</p> <p>1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after PCH_PWROK is high. Software will not be able to clear the Top Swap bit until the system is rebooted. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). This signal is in the primary well.
GPP_B18 / GSPiO_MOST	No Reboot	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = Disable "No Reboot" mode. (Default)</p> <p>1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after PCH_PWROK is high. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)</p> <p>1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after RSMRST# de-asserts. This signal is in the primary well.

TOP SWAP OVERRIDE STRAP

The signal has a weak internal pull-down.

0 = Disable "Top Swap" mode. (Default)

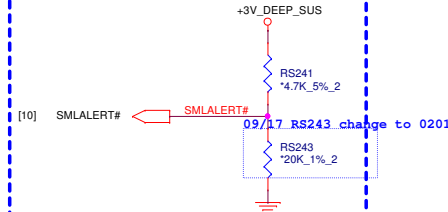
1 = Enable "Top Swap" mode. This inverts an address

**TLS CONFIDENTIALITY ENABLED**

This signal has a weak internal pull-down.

0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

**NO REBOOT IF SAMPLED HIGH**

The signal has a weak internal pull-down.

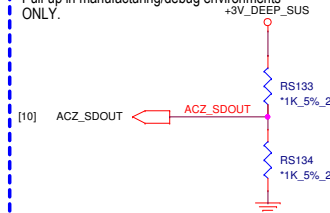
0 = Disable "No Reboot" mode. (Default)

1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

This signal has a weak internal pull-down.

0 = Enable security measures defined in the Flash Descriptor. (Default)

1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.



Pin Straps (Sheet 3 of 4)

Signal	Usage	When Sampled	Comment
SPiO_I03	Reserved	Rising edge of RSMRST#	<p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
HDA_SDO / I2SDO_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Enable security measures defined in the Flash Descriptor. (Default)</p> <p>1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after PCH_PWROK is high. This signal is in the primary well.
GPP_H12 / SMLALERT#	eSPI Flash Sharing Mode	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = Master Attached Flash Sharing (MAFS) enabled. (Default)</p> <p>1 = Slave Attached Flash Sharing (SAFS) enabled.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after RSMRST# de-asserts. This signal is in the primary well. <p>Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled)</p>
GPP_I16 / DDPB_C-TRLDATA	Display Port B Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port B is not detected. (Default)</p> <p>1 = Port B is detected.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after PCH_PWROK de-asserts. This signal is in the primary well.
GPP_I18 / DDPC_C-TRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port C is not detected. (Default)</p> <p>1 = Port C is detected.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after PCH_PWROK de-asserts. This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port D is not detected. (Default)</p> <p>1 = Port D is detected.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after PCH_PWROK de-asserts. This signal is in the primary well.
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port F is not detected. (Default)</p> <p>1 = Port F is detected.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after PCH_PWROK de-asserts. This signal is in the primary well. This strap applies to platforms that support Display Port F only. Refer to the platform's processor documentation for info on Display Port F support.

Pin Straps (Sheet 4 of 4)

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.</p> <p>0 = 38.4 MHz XTAL frequency selected. (Default)</p> <p>1 = 24MHz XTAL frequency selected.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after RSMRST# de-asserts. This signal is in the primary well.
GPP_J6 / CNV_RGL_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	<p>An external pull-up or pull-down is required.</p> <p>0 = Integrated CNVi enable.</p> <p>1 = Integrated CNVi disable.</p>
GPP_J9	1.8V VCCSPI	Rising edge of RSMRST#	<p>The signal has a weak internal pull-down</p> <p>0 = VCCSPI is connected to 3.3V rail</p> <p>1 = VCCSPI is connected to 1.8V rail</p> <p>Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os.</p>
GPd7	Reserved	Rising edge of DSW_PWROK	<p>External pull-up is required. Recommend 100K.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling</p>

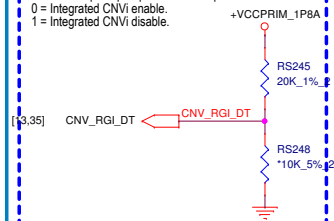
Matt change power source to +VCCPRIM_1P8A/0731

M.2 CNVi Mode Select

An external pull-up or pull-down is required.

0 = Integrated CNVi enable.

1 = Integrated CNVi disable.

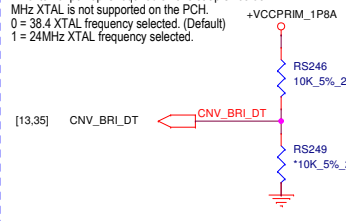
**XTAL Frequency Select**

This signal has a weak internal pull-down.

An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.

0 = 38.4 MHz XTAL frequency selected. (Default)

1 = 24MHz XTAL frequency selected.

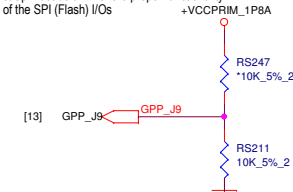
**GPP_J9 1.8V VCCSPI:**

The signal has a weak internal pull-down

0 = VCCSPI is connected to 3.3V rail

1 = VCCSPI is connected to 1.8V rail

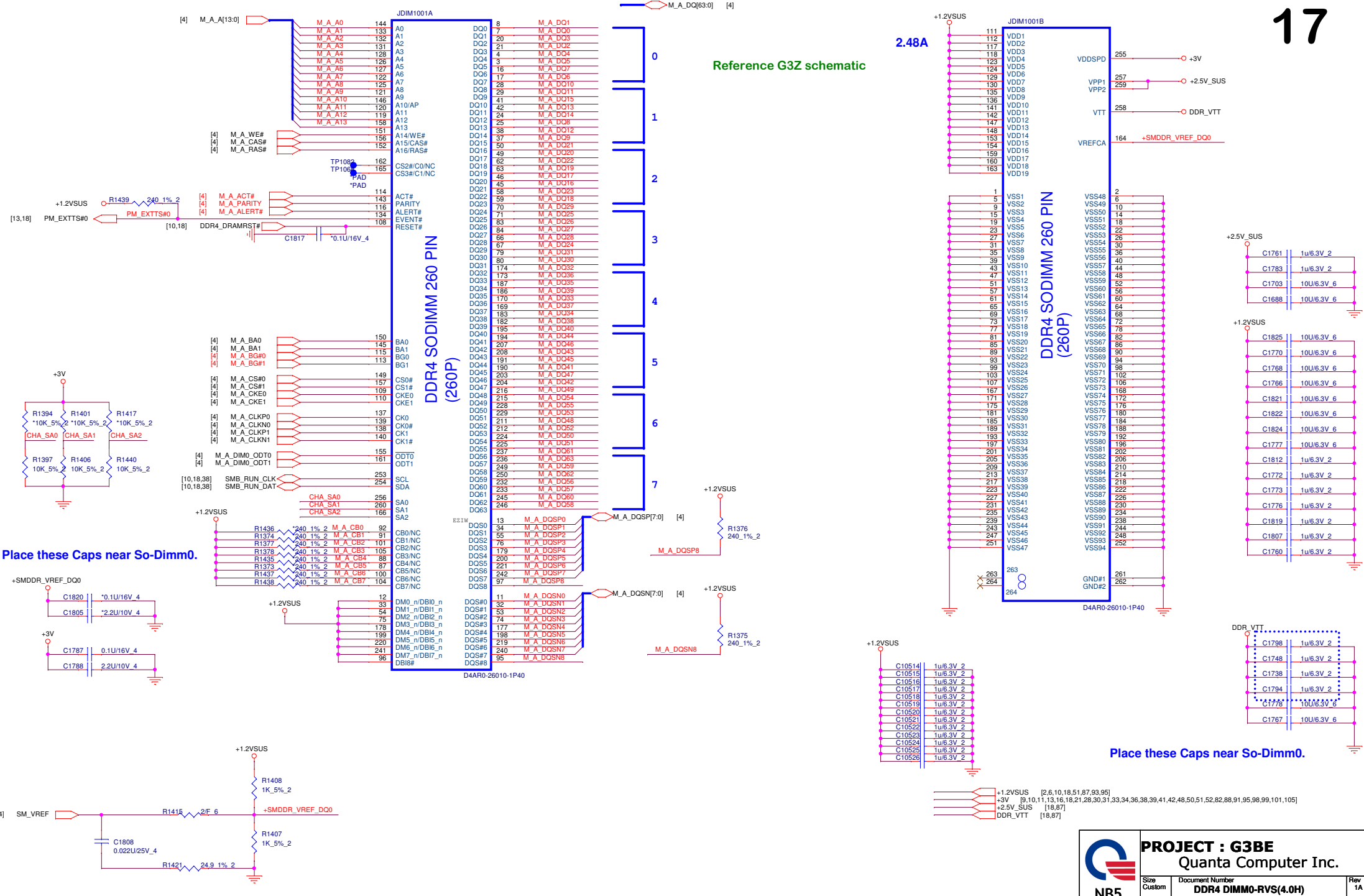
Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os



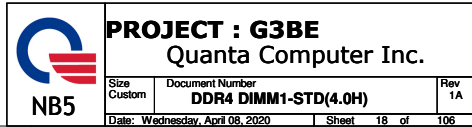
PROJECT : G3BE
Quanta Computer Inc.

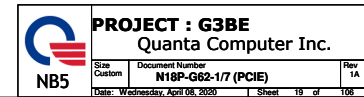
Size	Document Number	Rev
Custom	APS	1A
Date: Wednesday, April 08, 2020	Sheet 16 of 106	

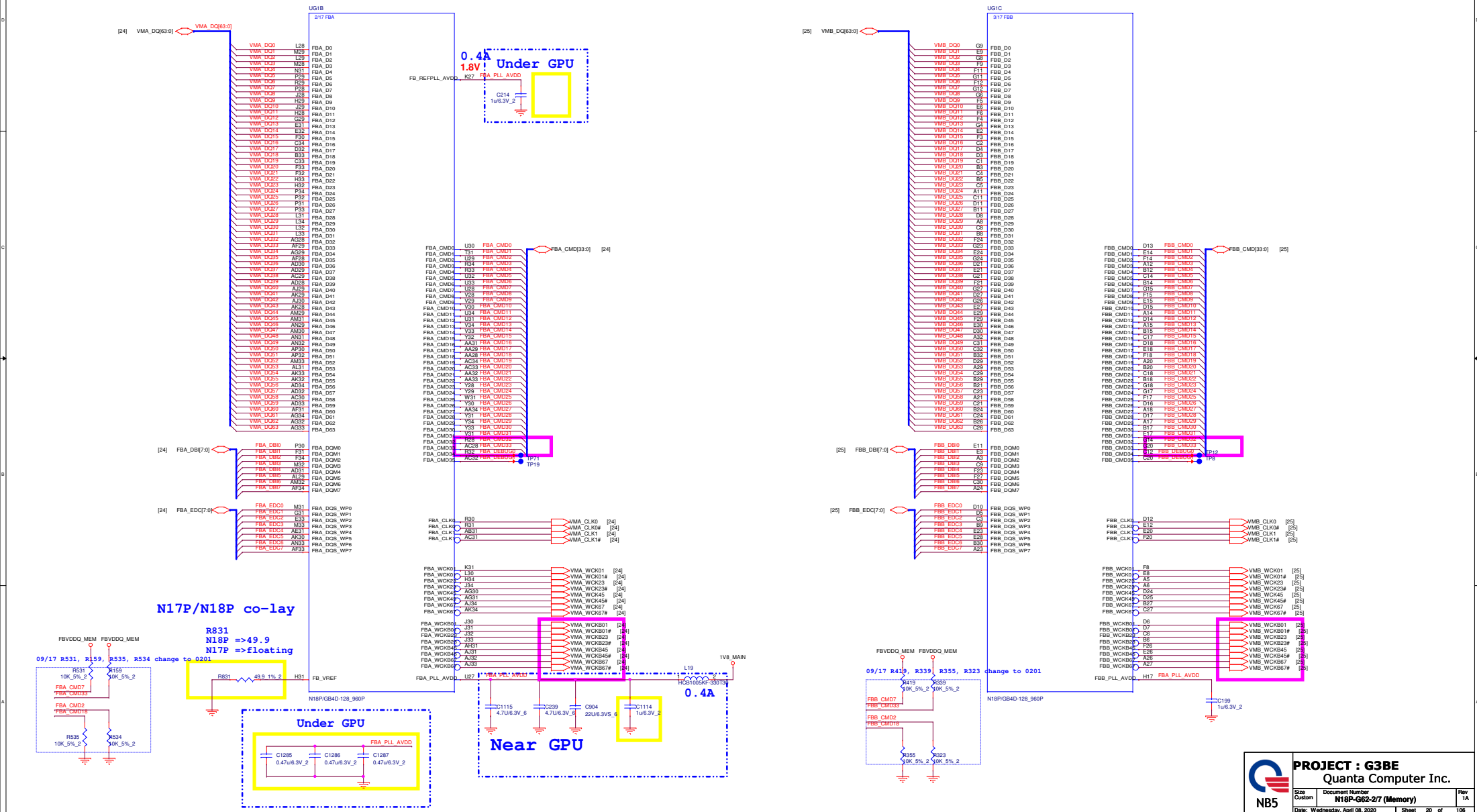
Reference G3Z schematic



Place these Caps near So-Dimm0.







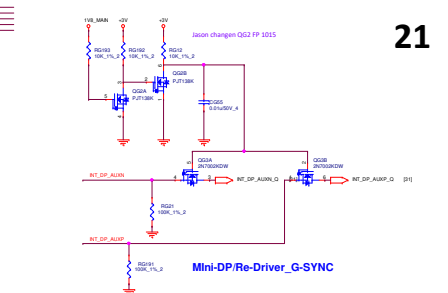
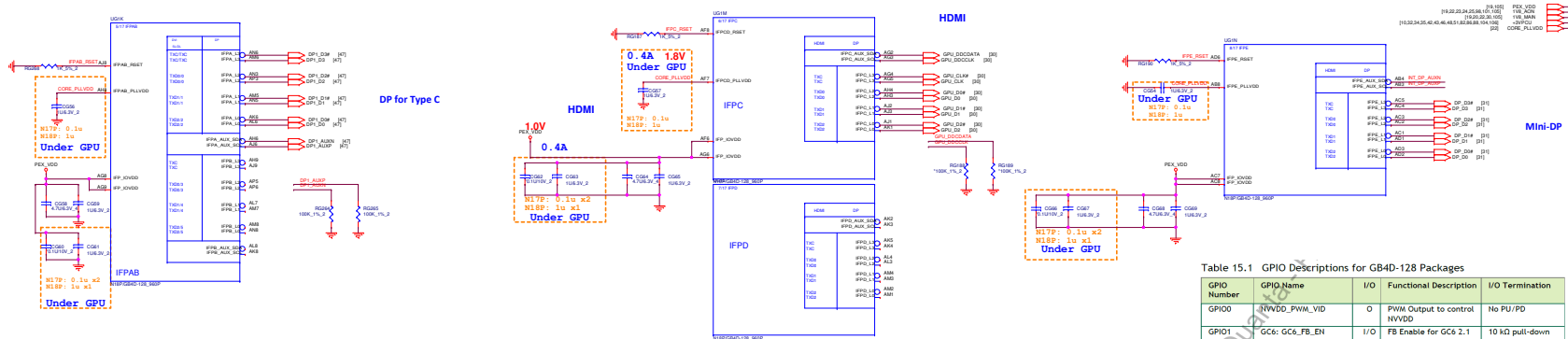


Table 15.1 GPIO Descriptions for GB4D-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVDD_PWM_VID	O	PWM Output to control NVDD	No PU/PD
GPIO1	GC6_GC6_FB_EN	I/O	FB Enable for GC6 2.1	10 kΩ pull-down

Table 15.1 GPIO Descriptions for GB4D-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO2	GC6_GPU_EVENT	I/O	GPU wake signal for GC6 2.1	10 kΩ pull-up to 1V8_AGN, unless driven actively.
GPIO3	UNUSED	O		
GPIO4	GC6_1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	10 kΩ pull-up to 1V8_AGN
GPIO5	FRAME_LOCK*	O	Active low Frame Lock	10 kΩ pull-up to 1V8_AGN
GPIO6	NVDD_PSI*	O	Phase Shedding (see section 15.3.3)	10 kΩ pull-up to 1V8_AGN to enable multiple phases
GPIO7	LCD_RL_PWM	O	LCD Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT*	I	Active Low Thermal Alert	100 kΩ pull-up to 1V8_AGN
GPIO10	MEM_VREF_CTL	O	Memory VREF control	100 kΩ pull-down
GPIO11	LCD_VDD	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	10K Pull Up
GPIO13	UNUSED			
GPIO14	HPD_IPFA*	I	Hot Plug Detect for IPFA	10K Pull Up to 1V8_AGN
GPIO15	HPD_IPFB*	I	Hot Plug	10K Pull Up to 1V8_AGN
GPIO16	UNUSED			
GPIO17	HPD_IPFD*	I	Hot Plug Detect for IPFD	10K Pull Up to 1V8_AGN
GPIO18	HPD_IPFE*	I	Hot Plug Detect for IPFE	10K Pull Up to 1V8_AGN
GPIO19	UNUSED	O		
GPIO20	GC6_INB_GC6	I/O		10K Pull Down
GPIO21	LCD_BLEN	O	LCD Panel Backlight enable	100K Pull Down
GPIO22	INA_HTT* / ADC_MUX_SEL	O	2.2K Pull Up See circuit	100K Pull Down
GPIO23	Reserved			
GPIO24	UNUSED			
GPIO25	FBVDD_PSI*	I	PU/PD with series resistor depending on PSI topology	100 kΩ pull-down
GPIO26	FP_FUSE			
GPIO27	HPD_IPFC*	I	Hot Plug detect for IFPC	10K Pull Up to 1V8_AGN

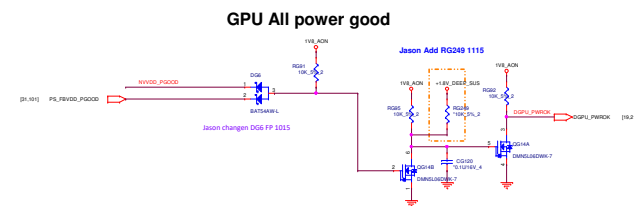
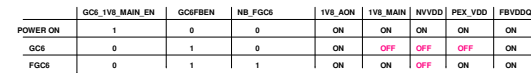
VRAM Table for G1/G2 GDDR6

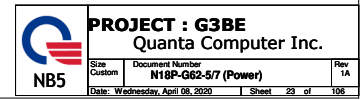
Vendor	Vendor P/N	TOP P/N	GB P/N
SK Hynix	M161X256M32E-14-A	Y80	A200505103
Samsung	K4D8328BC-HE14	Y80	A200505103

Table 5.3 RAMCFG			
Strap Pins (see Note)			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory NVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H ₀	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)

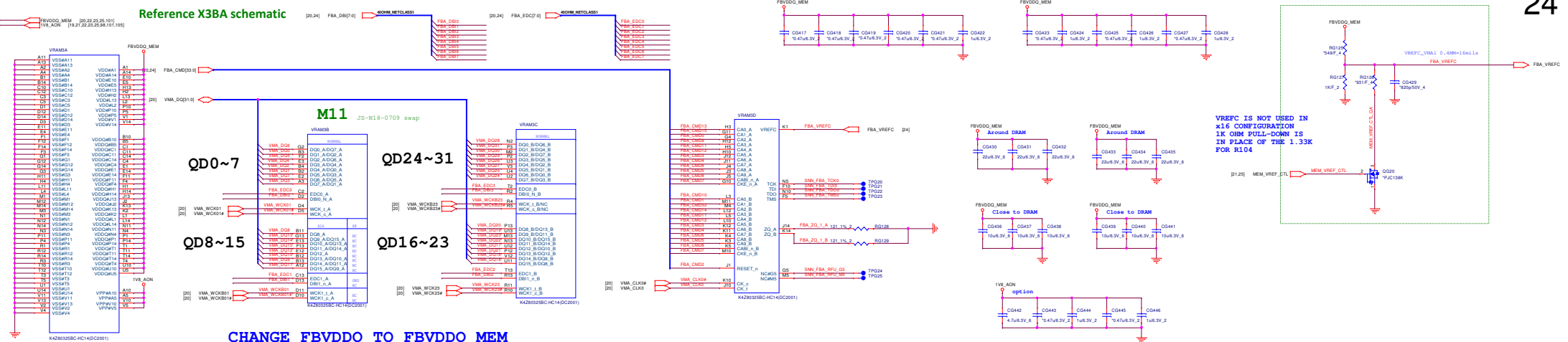


If N18P only, connect these pin to GND
If N17P/N18P co-layout, leave these pin NC
If N17P only, leave these pin NC

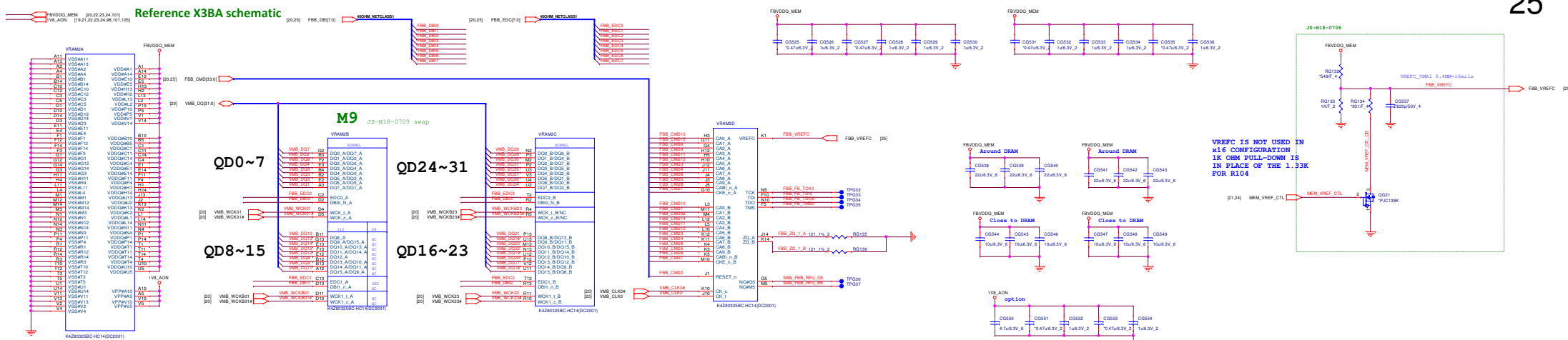




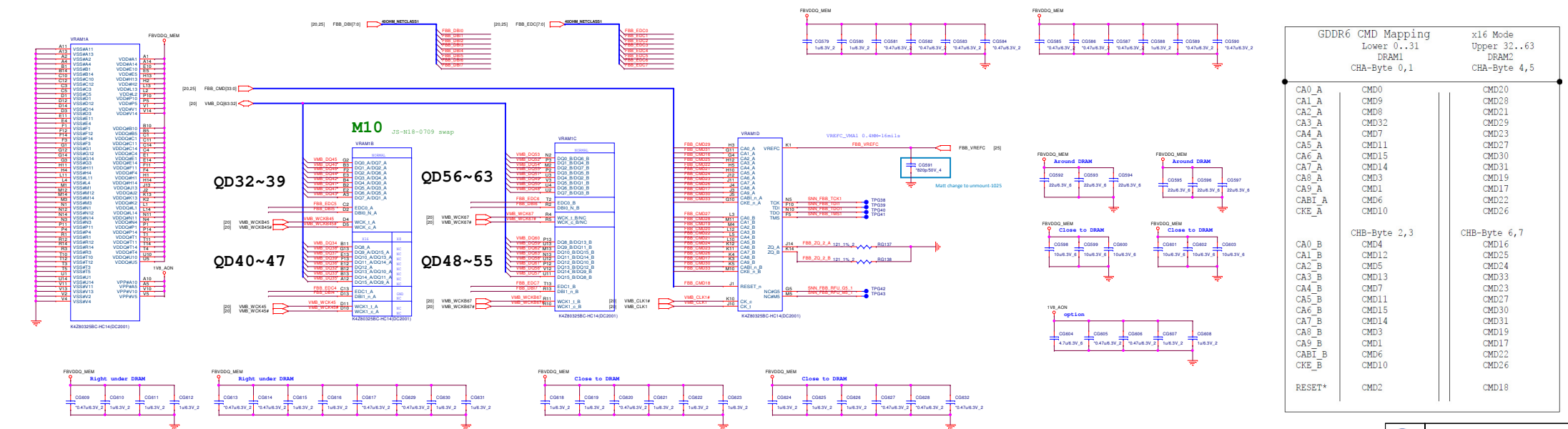
MEMORY: FBA Partition 31..1.0



MEMORY: FBB Partition 31..0

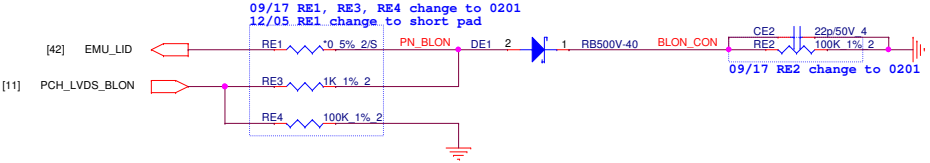


MEMORY: FBB Partition 63..32

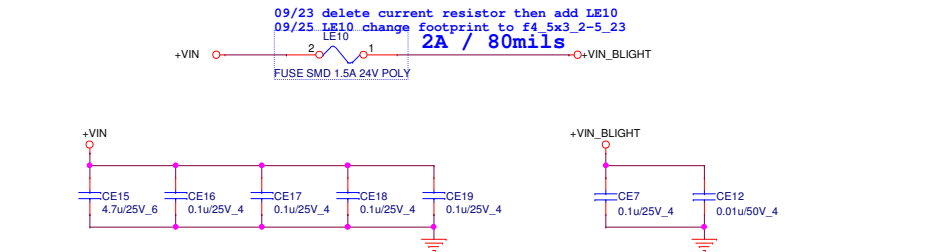


LID Switch

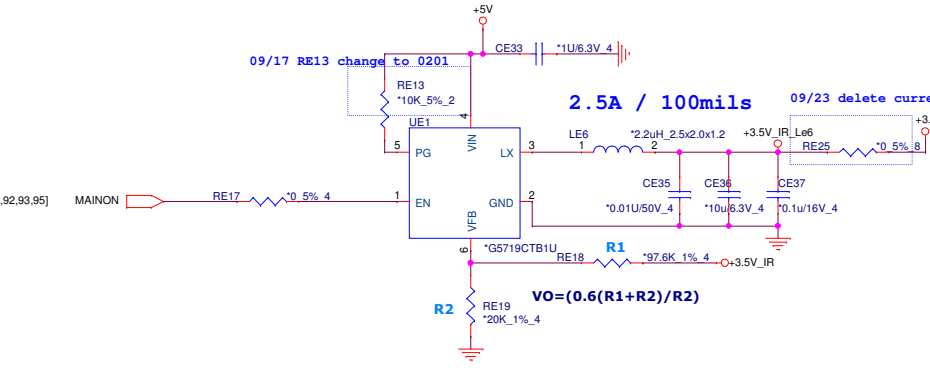
Reference G3DC schematic



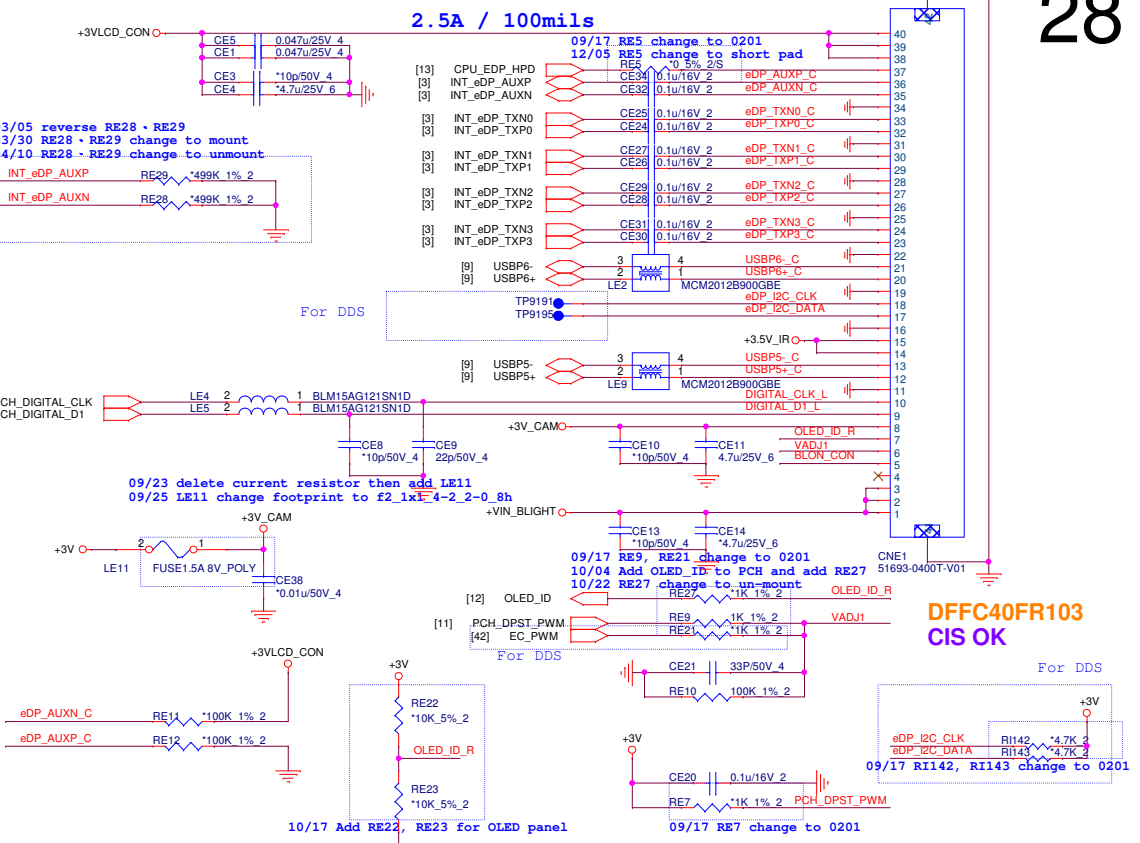
LCD Blight



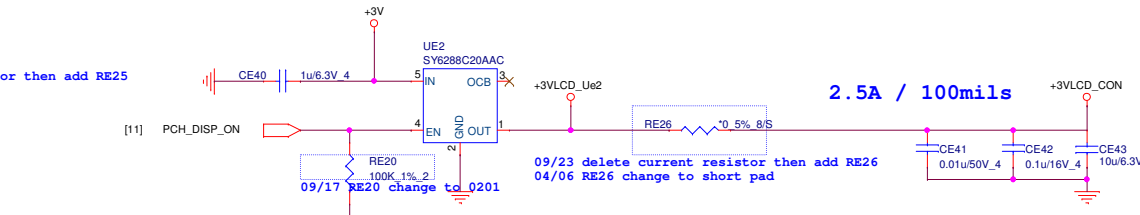
IR CAM Power SW

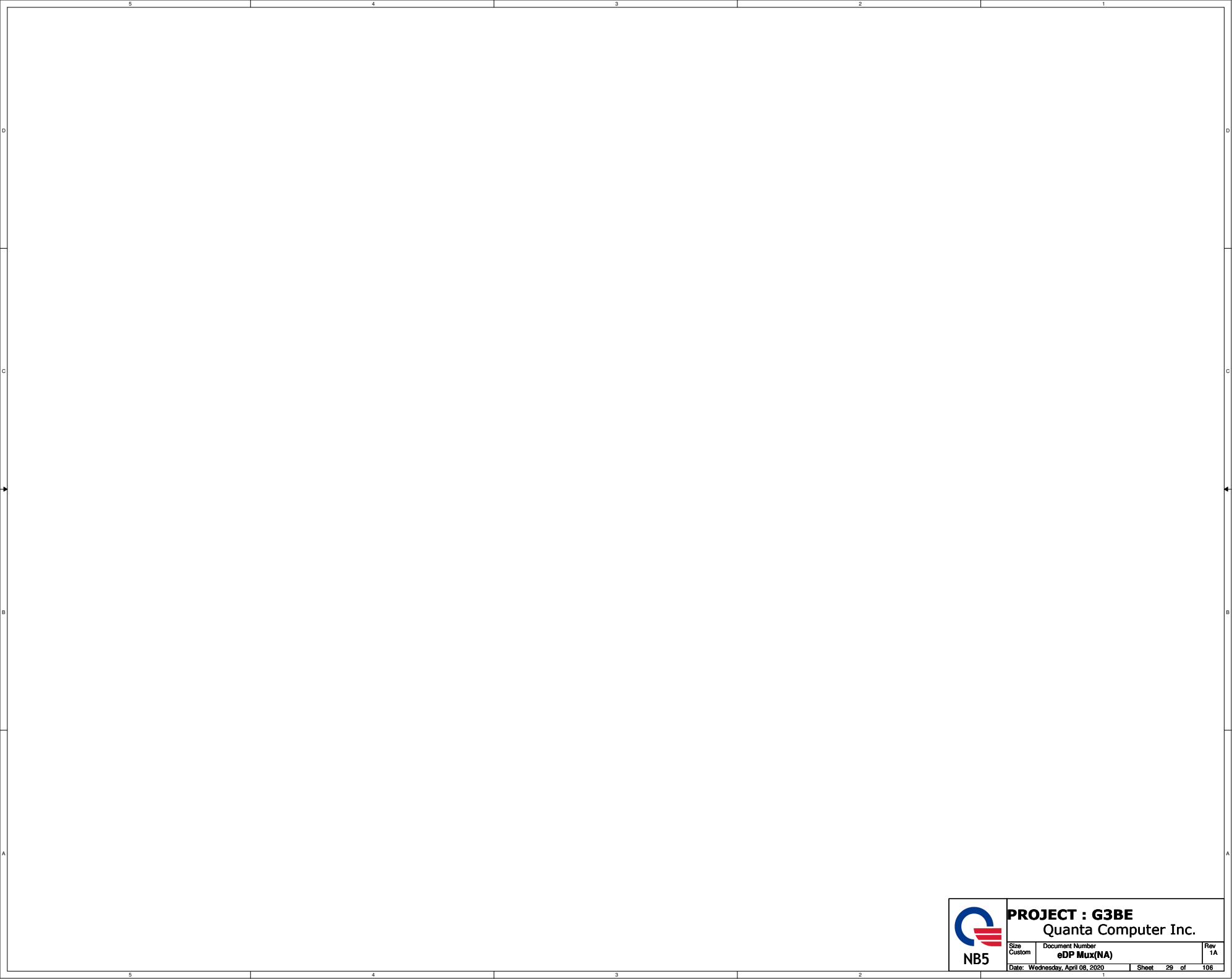


eDP Conn.

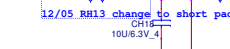
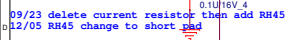


3V LCD Power SW





3



BAM10120003 - Ciss = 60pF, MAX Vgs = 1.0V
if DDC test fail, Change to BAM84060000 - Ciss = 35pF, MAX Vgs = 1.0V

Debug & Flash FW BAM70020021 - Ciss Under 15pF

1V8_MAIN RH28 10K 5% 2

GPU_DDCCLK

GPU_DDCDATA

1V8_MAIN RH33 10K 5% 2

PMG1012T-7

PMG1012T-7

SCL_SINK_C

SDA_SINK_C

SCL_SINK

SDA_SINK

+OVDD33

RH35 0.5% 2

RH38 10K 5% 2

RH39 22 1% 2

RH40 22 1% 2

RH41 22 1% 2

RH42 22 1% 2

RH43 10K 5% 2

RH44 0.5% 2

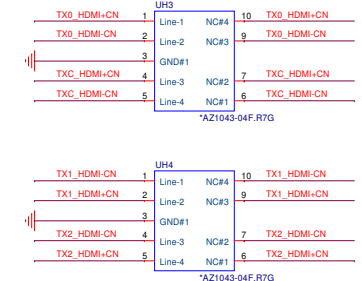
QH3 NX7002AKW

QH4 NX7002AKW

Diagram showing the pin connections for U4H3 (TX0_HDMI+CN). The component is a 10-pin device. The connections are as follows:

Pin	Signal	Internal Label
1	TX0_HDMI+CN	Line-1
2	TX0_HDMI+CN	NC#4
3	GND#1	NC#3
4	TXC_HDMI+CN	Line-3
5	TXC_HDMI-CN	NC#2
6	TXC_HDMI-CN	NC#1
7	TXC_HDMI+CN	Line-4
8	TXC_HDMI+CN	NC#1
9	TX0_HDMI-CN	NC#3
10	TX0_HDMI-CN	NC#4

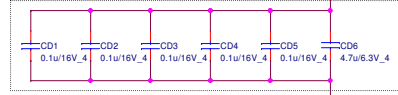
*A2I043-04F.R7G



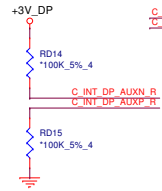
DFHD19MR641
CIS OK

+3VSS [10,12,14,23,35,38,42,47,48,51,82,86,88,92,93,95,104,105]
 +3V [9,10,11,13,16,17,18,21,28,30,33,34,36,38,39,41,42,46,50,51,52,82,88,91,95,98,99,101,105]
 +5V [28,30,38,39,48,49,50,51,52,89,90,91,95,104]

Close to UD1 Chip



DisplayPort Source



C INT_DP_AUXP RD9 0.4S C INT_DP_AUXP_R 24
 C INT_DP_AUXN RD1 0.4S C INT_DP_AUXN_R 25
 01/21 RD9 - RD11 change to short pad

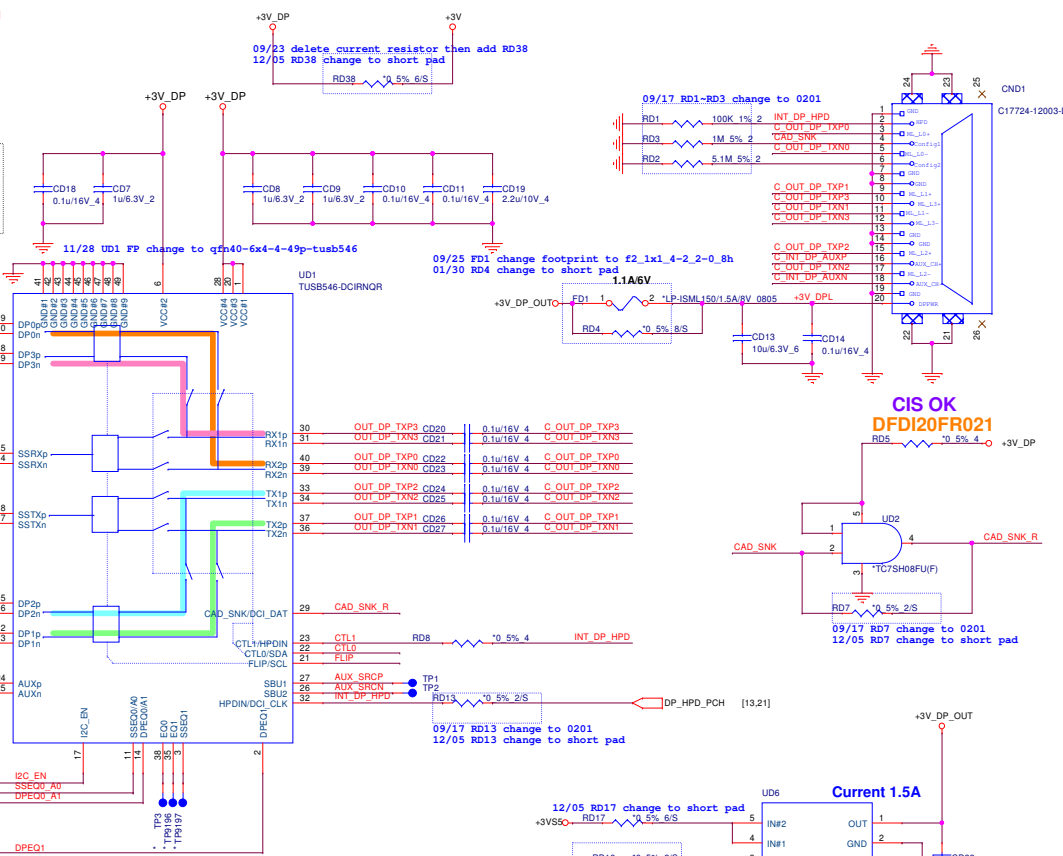
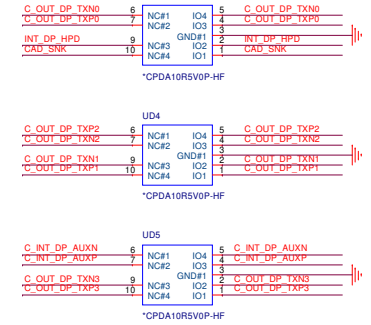


Table 2-1: Source-Side Mini DisplayPort Connector Pin Assignment

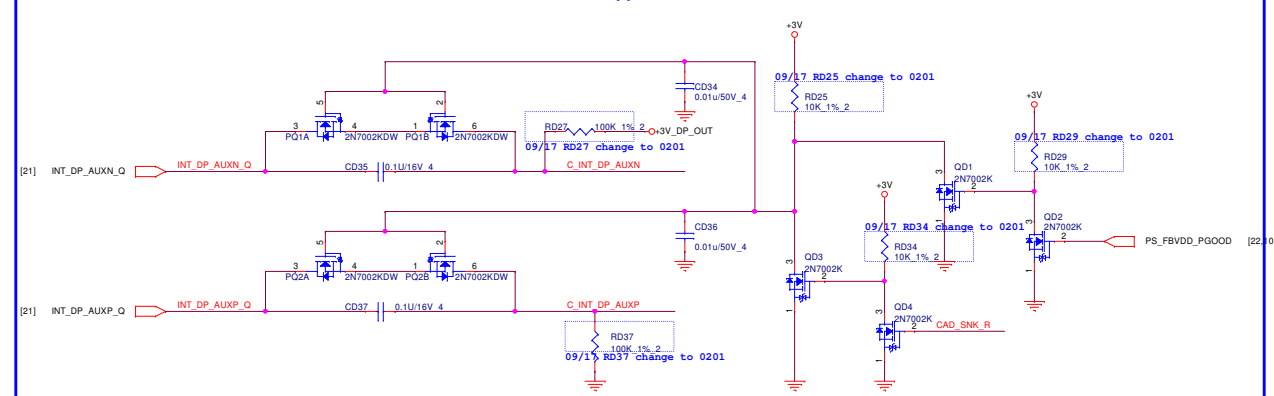
Top Row			Bottom Row		
Pin Number	Signal Type	Pin Name	Pin Number	Signal Type	Pin Name
1	GND	GND	2	In	Hot Plug Detect
3	Out	ML_Lane 0 (p)	4	CONFIG (see note 1)	CONFIG1
5	Out	ML_Lane 0 (n)	6	CONFIG (see note 1)	CONFIG2
7	GND	GND	8	GND	GND
9	Out	ML_Lane 1 (p)	10	Out	ML_Lane 3 (p)
11	Out	ML_Lane 1 (n)	12	Out	ML_Lane 3 (n)
13	GND	GND	14	GND	GND
15	Out	ML_Lane 2 (p)	16	I/O	AUX_CH (p)
17	Out	ML_Lane 2 (n)	18	I/O	AUX_CH (n)
19	GND	GND	20	PWR Out (see note 2)	DP_PWR

For ESD



Layout note: Place close to mini display Conn

Support dual mode



I2C Programming or pin strap programming select.
 I2C is only disable when this pin is '0'
 0 : Pin Strap (I2C disable) (Default)
 R : TI test mode (I2C enable at 3.3V)
 F : I2C enabled at 1.8V
 1 : I2C enabled at 3.3V

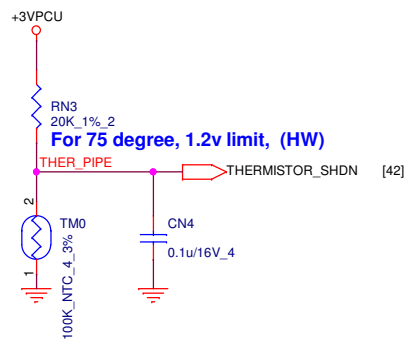
DPEQ0_A1 RD30 1K 5% 4
 RD31 1K 5% 4
 12/06 RD30, RD31, RD35, RD36 change to 0402 & RD36 change to mount
 DPEQ1 RD35 1K 5% 4
 RD36 1K 5% 4
 DPEQ0, DPEQ1 : DP Receiver equalization gain
 F,F (Default)
 When I2C_EN is not '0' DPEQ0 sets I2C address

SSEQ0, SSEQ1 : USB receiver equalizer gain
 for upstream facing SSTXP/N
 F,F (Default)
 When I2C_EN is not '0' SSEQ0 sets I2C address

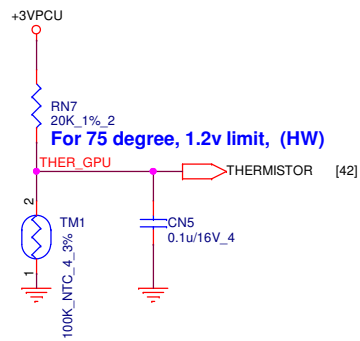
Reference G3Z schematic

Thermal Protect

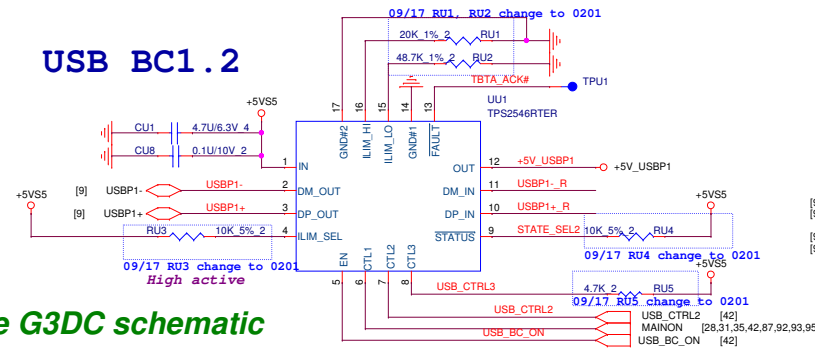
Under CPU pipe for travel bag test



CPU area to monitor CPU temp.

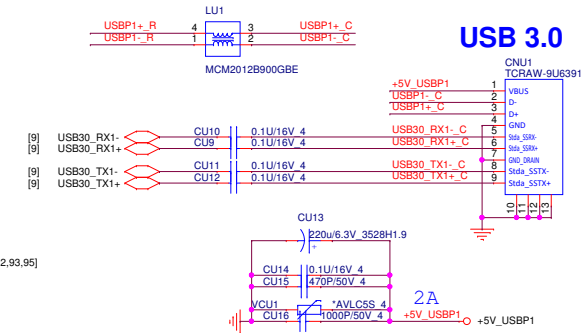


USB BC1.2

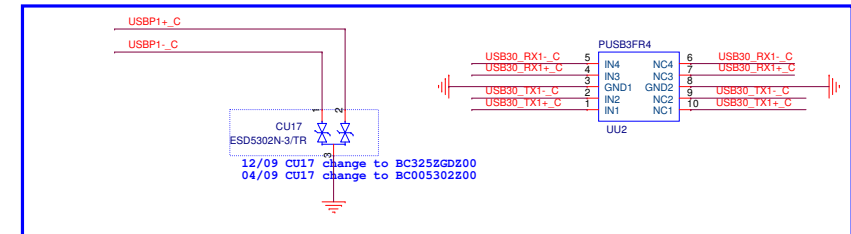


Reference G3DC schematic

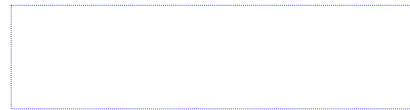
USB 3.0



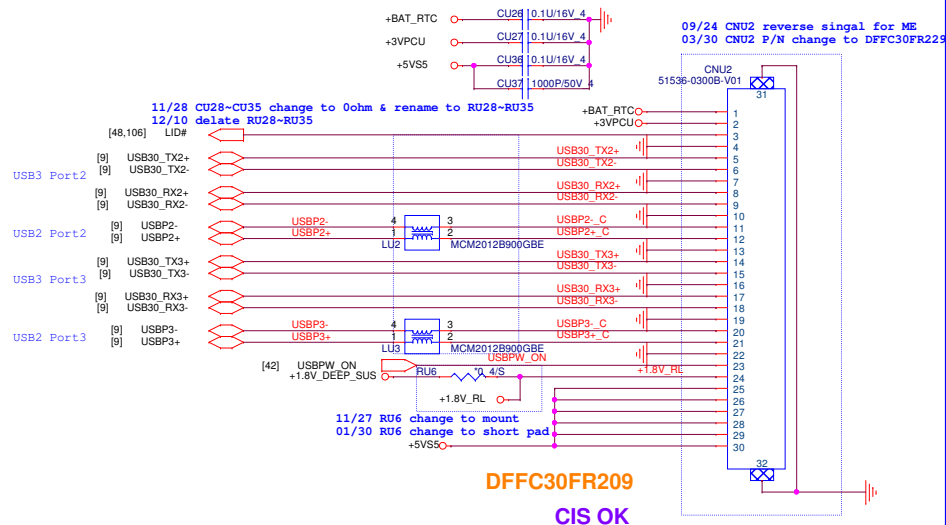
Place Back to Back La



USB3 small board

11/27 LU2 - LU3 change to unmount & add RU36-RU39
12/10 delete RU36-RU39

USB 2.0/3.0 Combo x2

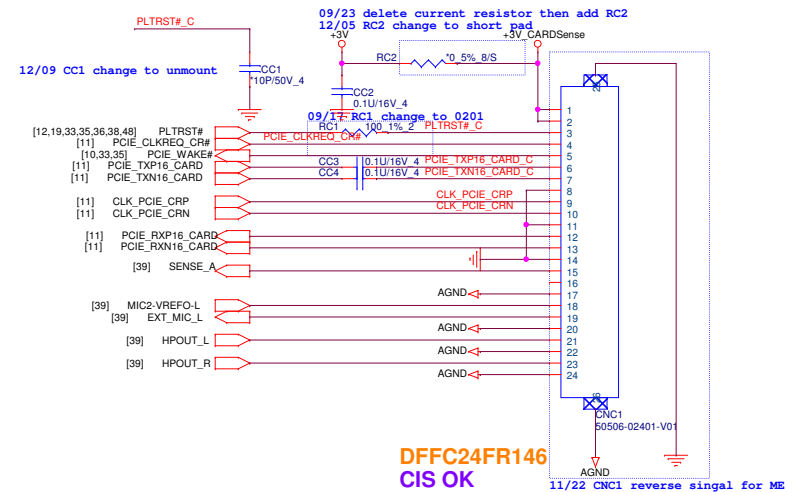


DFFC30FR209

CIS OK

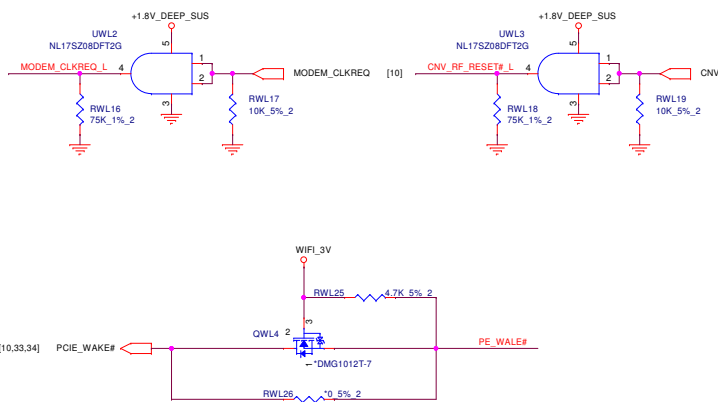
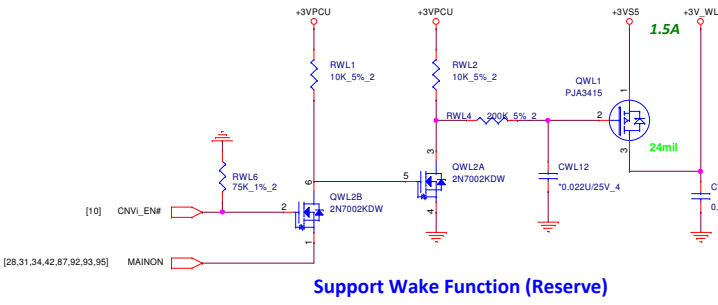
SD Card Audio Jack to Small Board

Reference G3DC schematic



DFFC24FR146

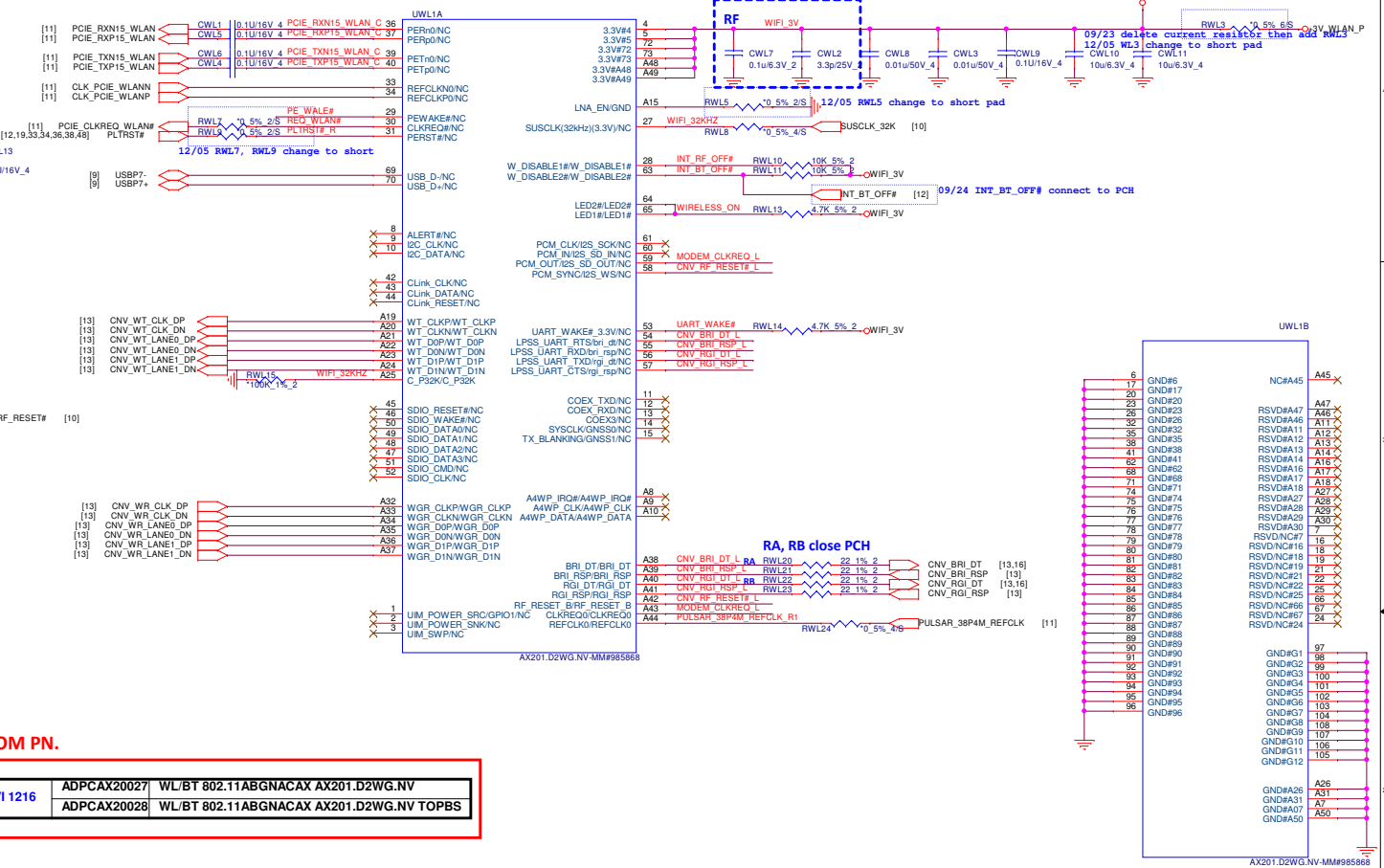
CIS OK



WLAN module BOM PN.

Harrison Peak 2 CNVI 1216	ADPCAX20027	WL/BT 802.11ABGNACAX AX201.D2WG.NV
	ADPCAX20028	WL/BT 802.11ABGNACAX AX201.D2WG.NV TOPBS

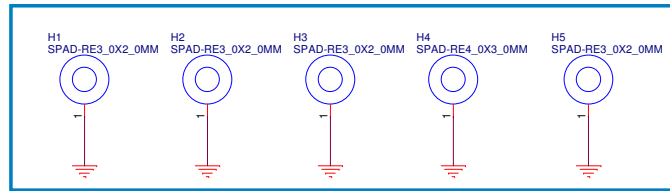
Reference G3Z schematic



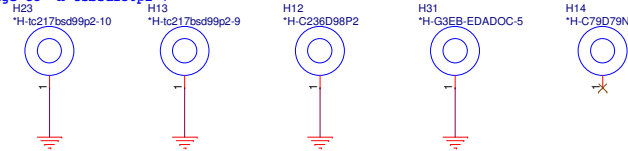


EMI PAD

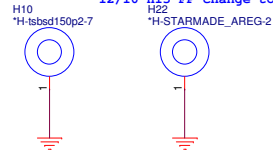
10/14 H1-H3 & H5 change to GBBLV004010
H4 change to GBTMA002010
10/15 H4 FP change to SPAD-RE4_0X3_0MM
10/16 H1-H3 & H5 FP change to SPAD-RE4_0X3_0MM



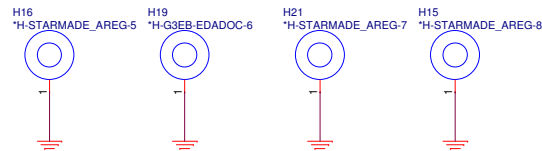
12/10 H23 FP change to H-tsbsd150p2-7



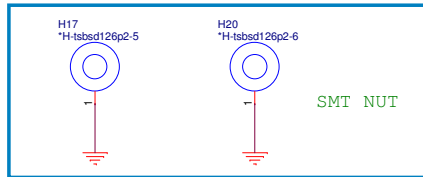
11/29 H13 FP change to SPAD-C237N
12/10 H13 FP change to H-tc217bsd99p2-9
12/06 H31 FP change to H-G3EB-EDADOC-5



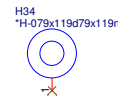
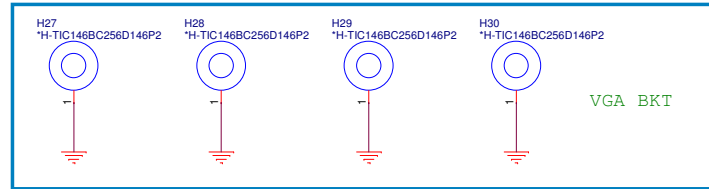
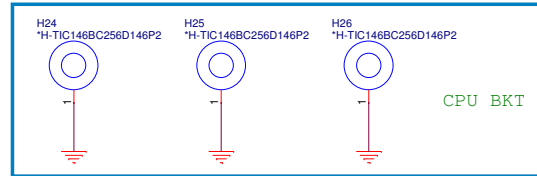
12/10 H10 FP change to H-tsbsd150p2-7



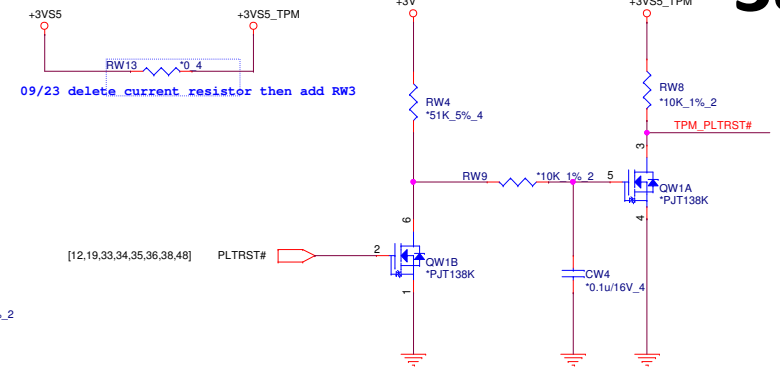
12/06 H19 FP change to H-G3EB-EDADOC-6



10/15 H17 FP change to HG-G3EB-EDADOC-1
H20 FP change to HG-G3EB-EDADOC-2
11/29 H17 FP change to HG-G3EB_C-EDADOC-1
H20 FP change to HG-G3EB_C-EDADOC-2
12/06 H17 FP change to H-G3EB-EDADOC-3 & change to unmount
H20 FP change to H-G3EB-EDADOC-4 & change to unmount
12/10 H17 FP change to H-tsbsd126p2-5
H20 FP change to H-tsbsd126p2-6



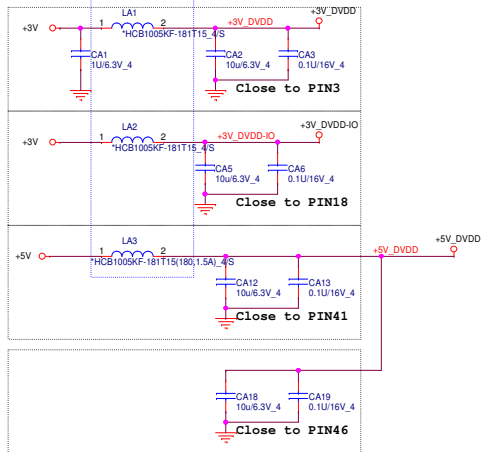
12/10 H34 FP change to H-079x119d79x119n



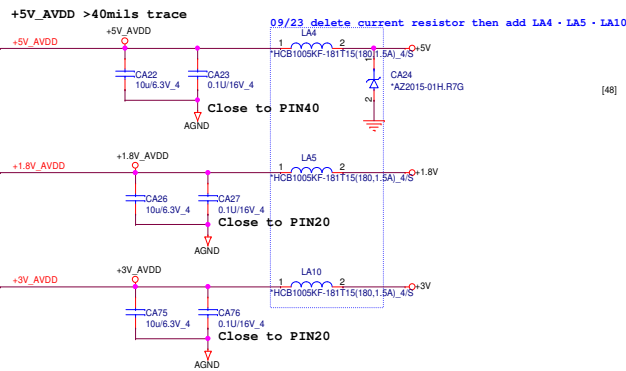
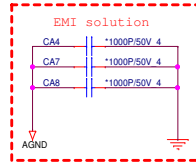
Size Custom	Document Number TPM/FAN/TP/Debug/IR Sensor	Rev 1A
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Reference G3Z

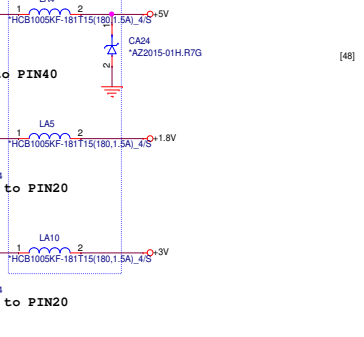
09/23 delete current resistor then add LA1 - LA2 - LA3



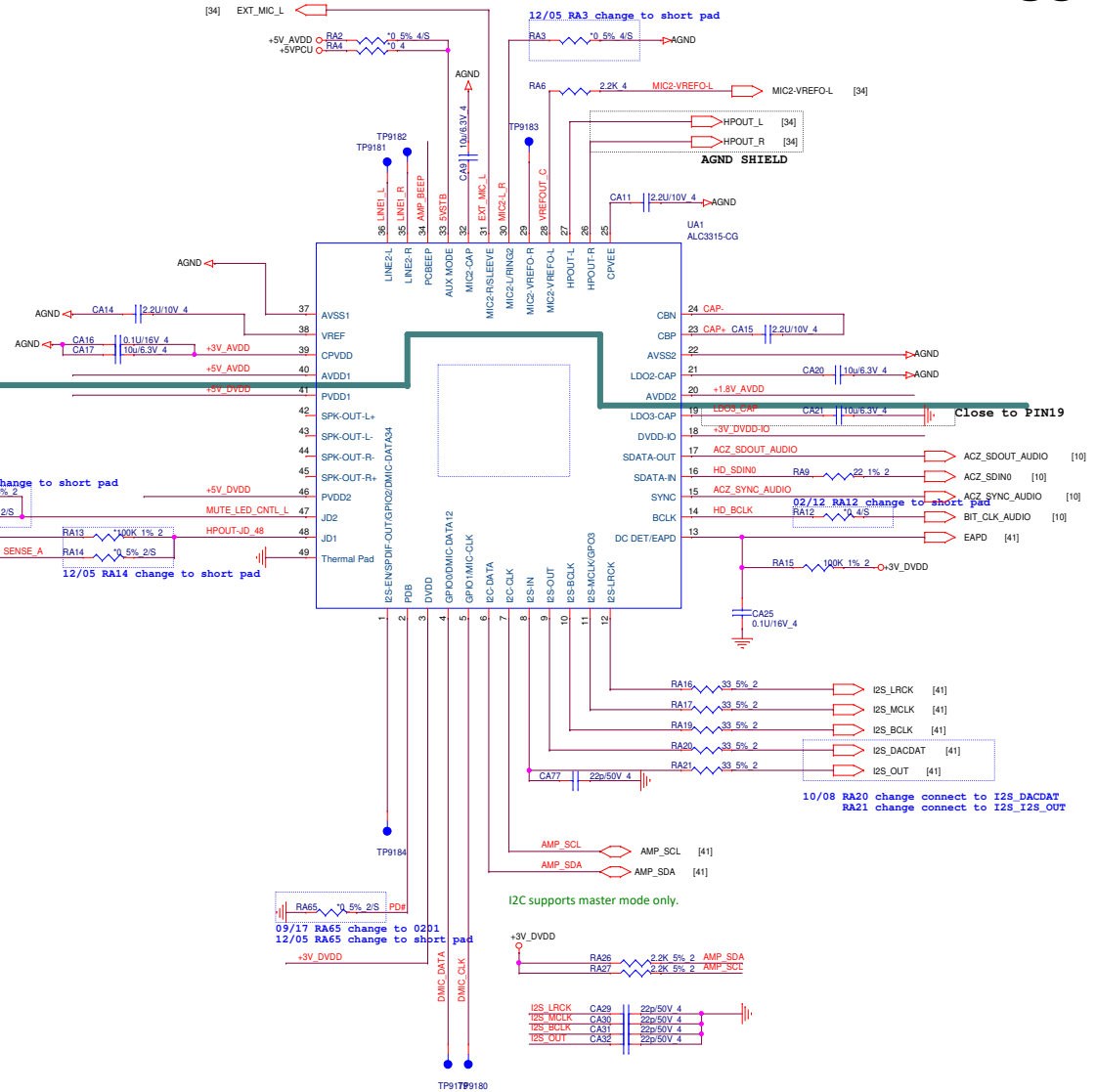
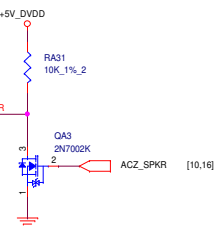
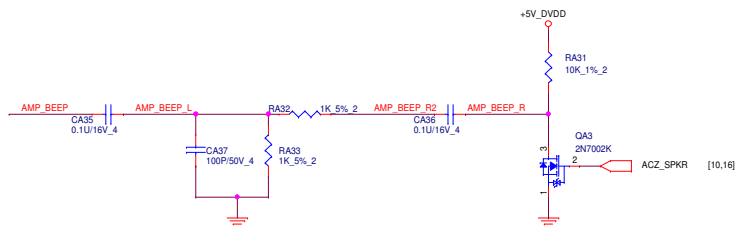
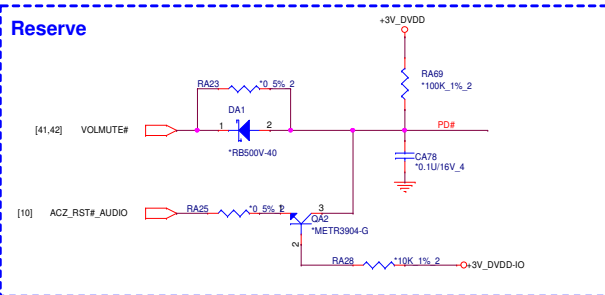
place to near or under codec



09/23 delete current resistor then add LA4 - LA5 - LA10



Reserve



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Quanta Computer Inc.

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CHECK WITH G3ZA
Head Phone out

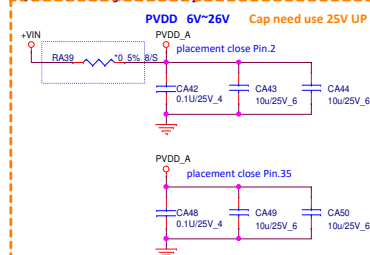
Head Phone jack

schematic reference X3A

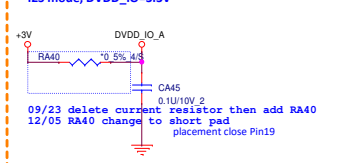
Speaker AMP

09/23 delete current resistor then add RA39

12/05 RA39 change to short pad



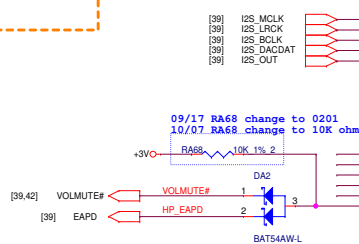
I2S mode, DVDD IO=3.3V



0.10/10V_2
09/23 delete current resistor then add RA40
12/05 RA40 change to short pad
placement close Pin19

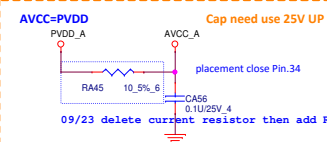
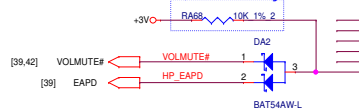
12/05 RA40 change to short pad
placement close Pin19

12/05 RA40 change to short pad
placement close Pin19

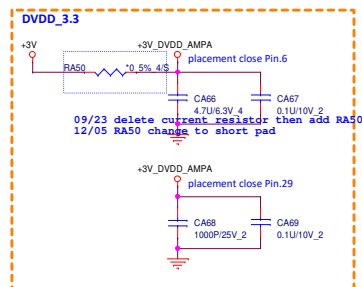


09/17 RA68 change to 0201
10/07 RA68 change to 10K ohm

10/07 RA68 change to 10K ohm

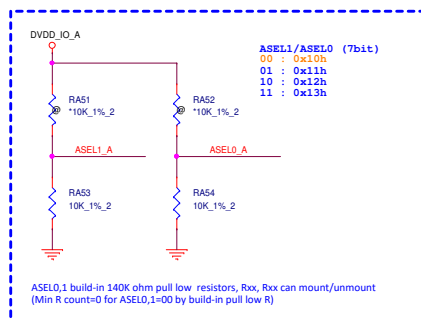


09/23 delete current resistor then add RA45

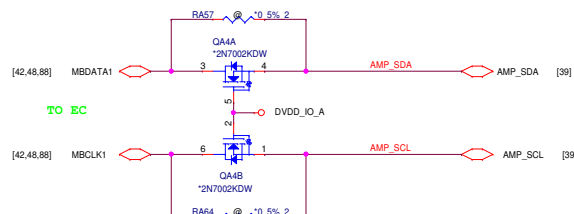


09/23 delete current resistor then add RA50
12/05 RA50 change to short pad

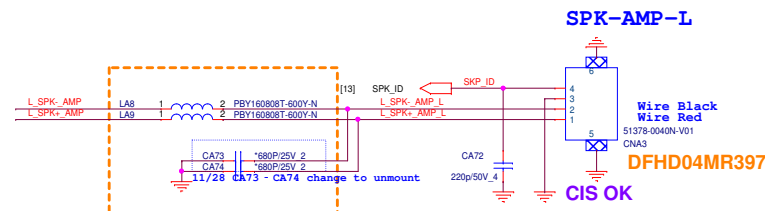
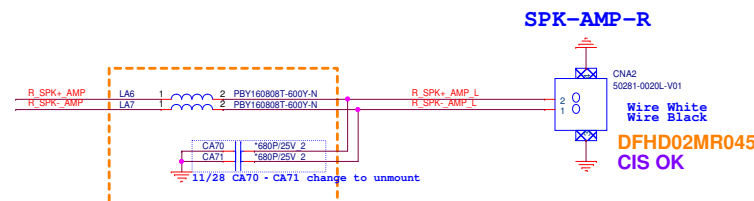
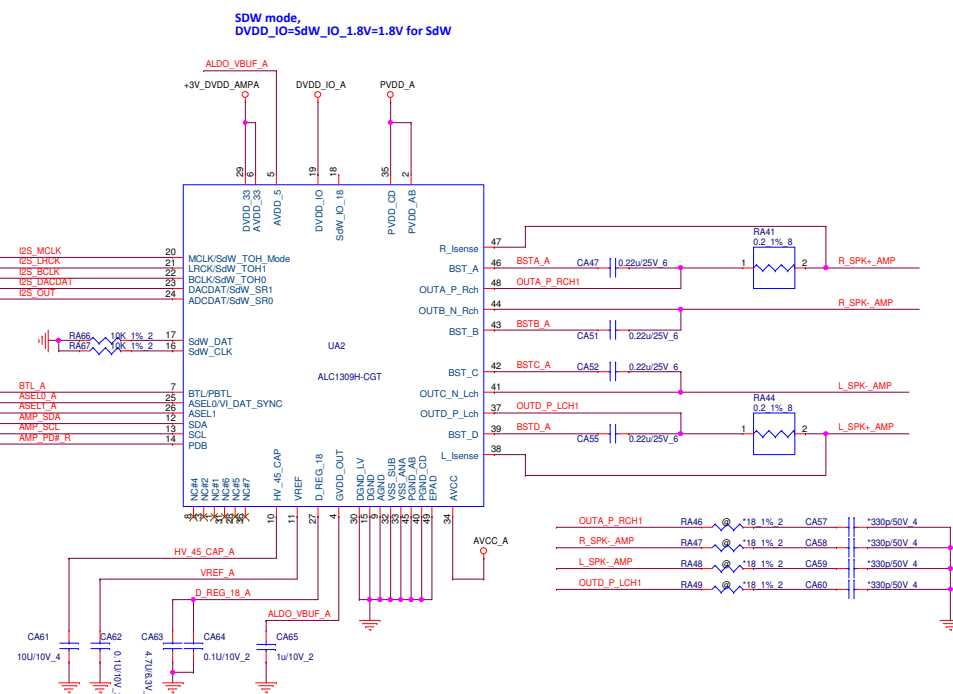
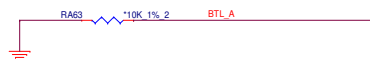
12/05 RA50 change to short pad



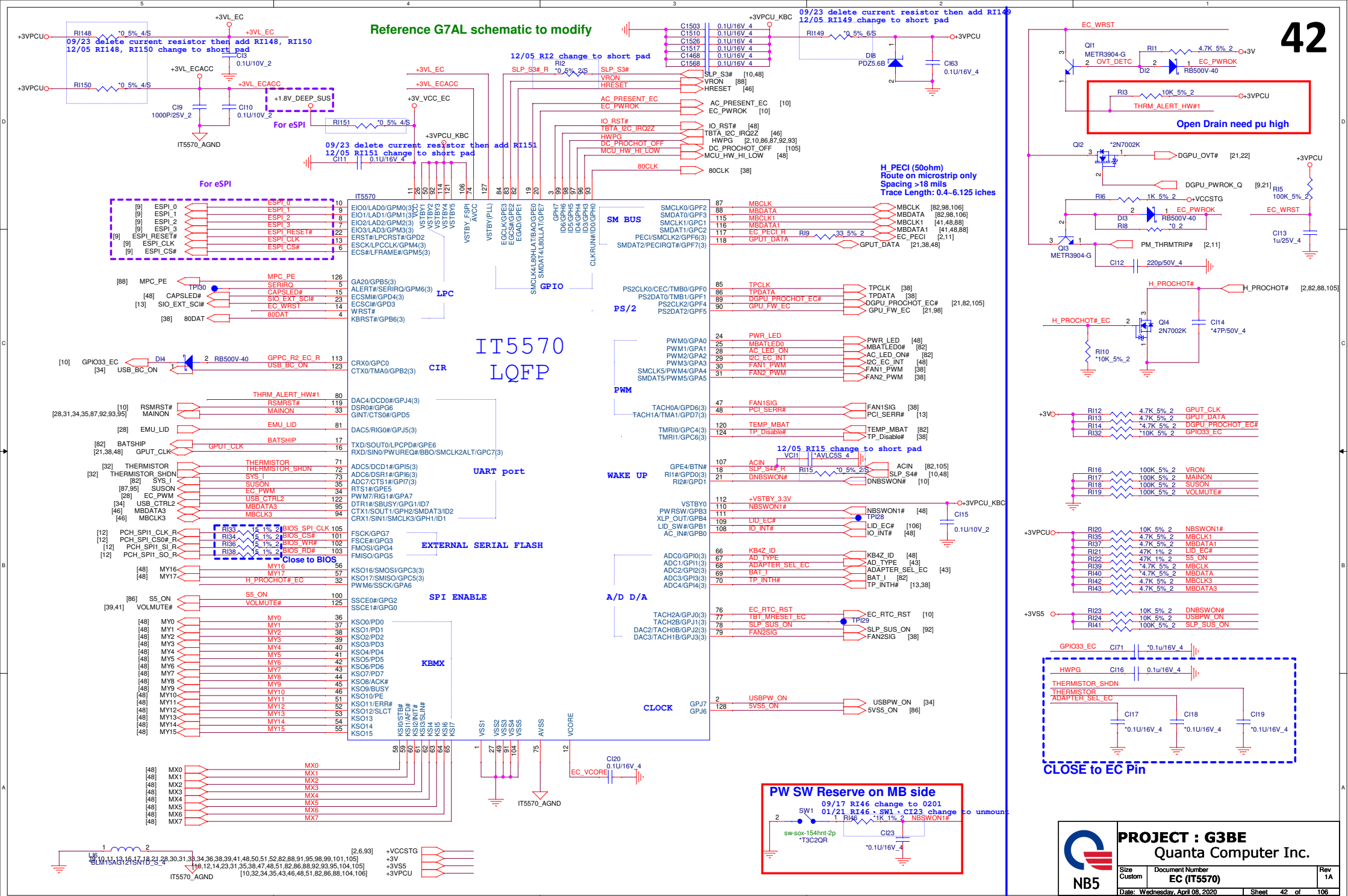
ASELO,1 build-in 140K ohm pull low resistors, Rxx, Rxx can mount/unmount
(Min R count=0 for ASELO,1=00 by build-in pull low R)



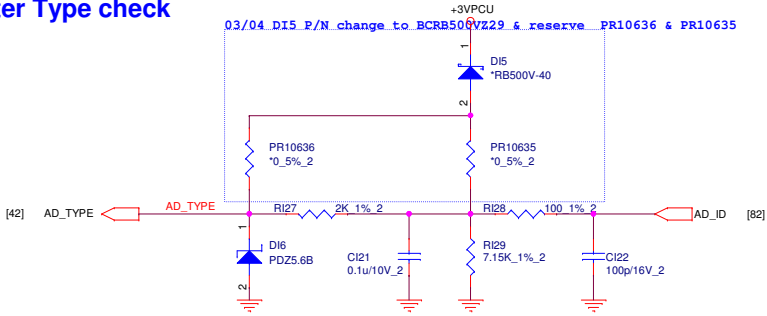
TO EC



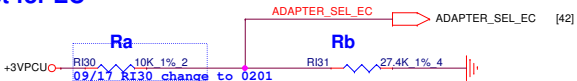
Reference G7AL schematic to modify



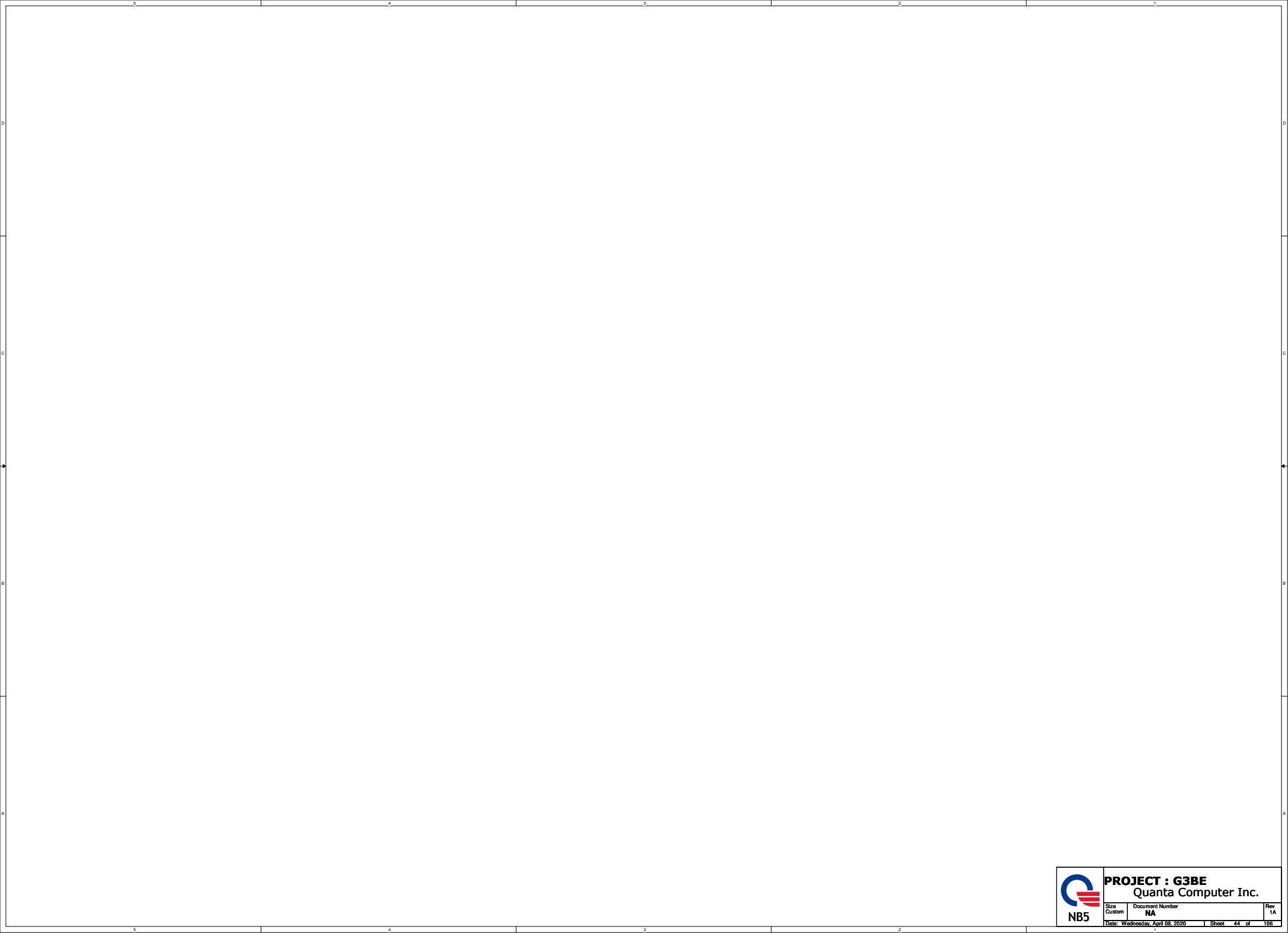
Adapter Type check




Adapter select for EC



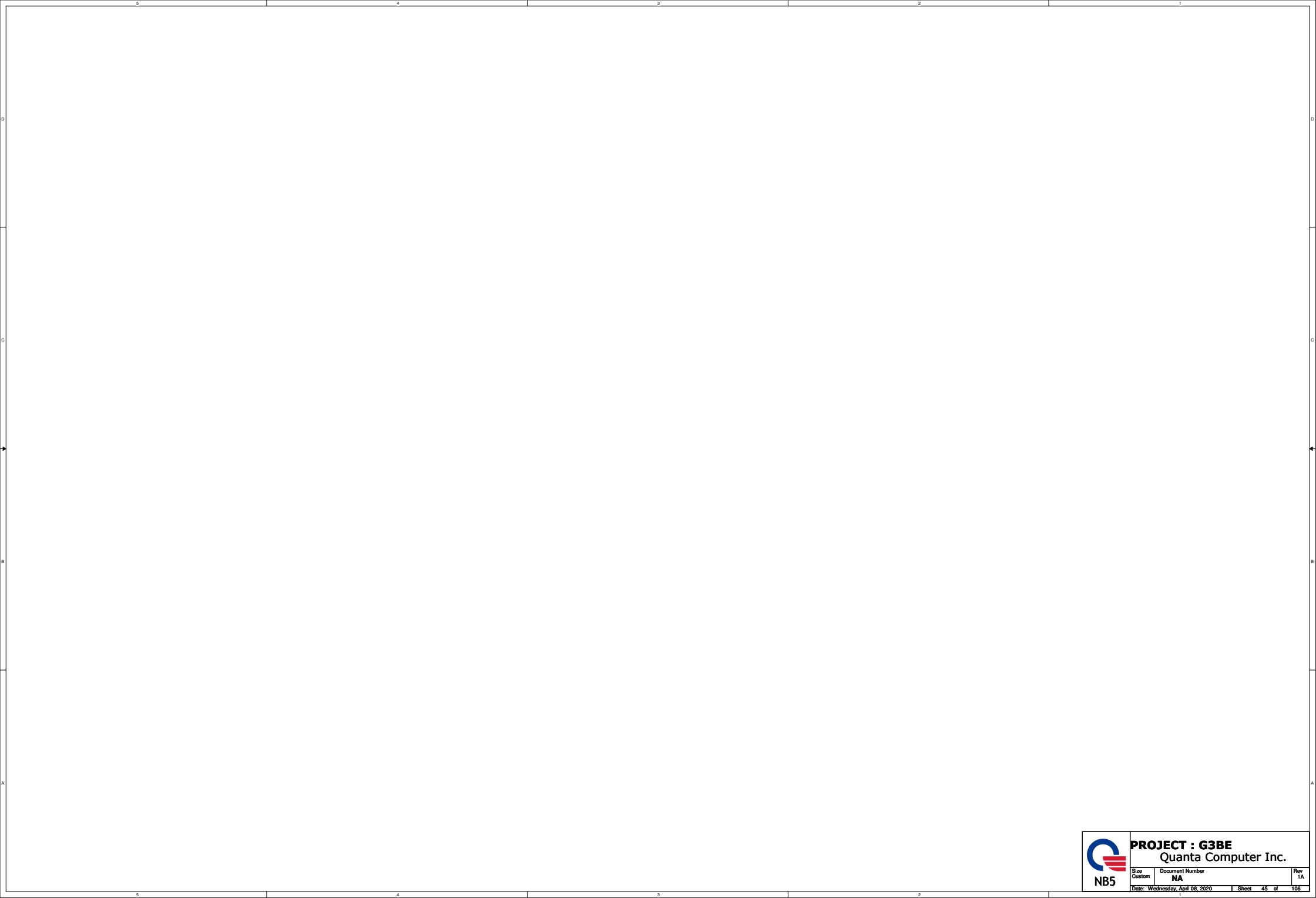
	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	N18E
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	2.42V	N18P



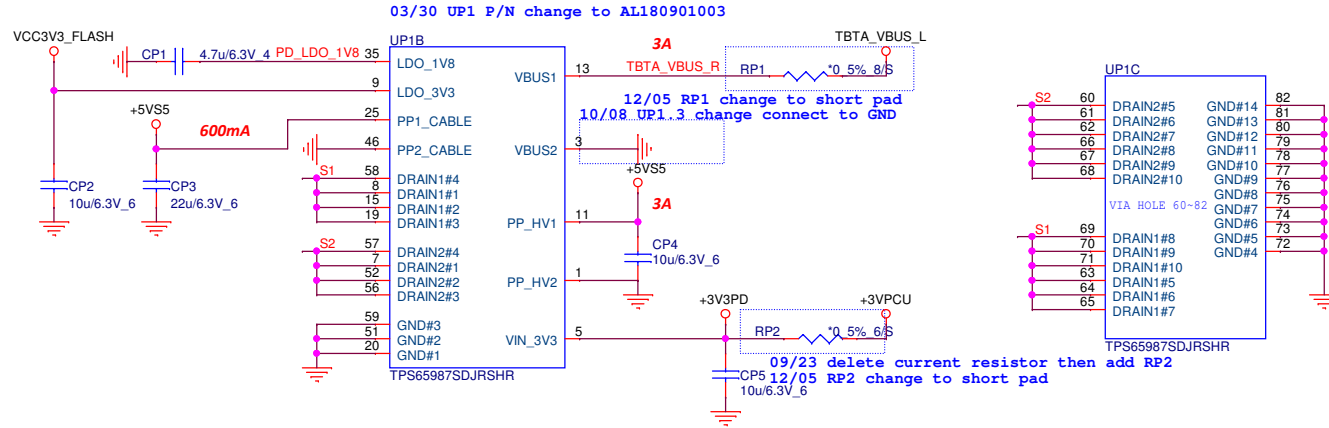


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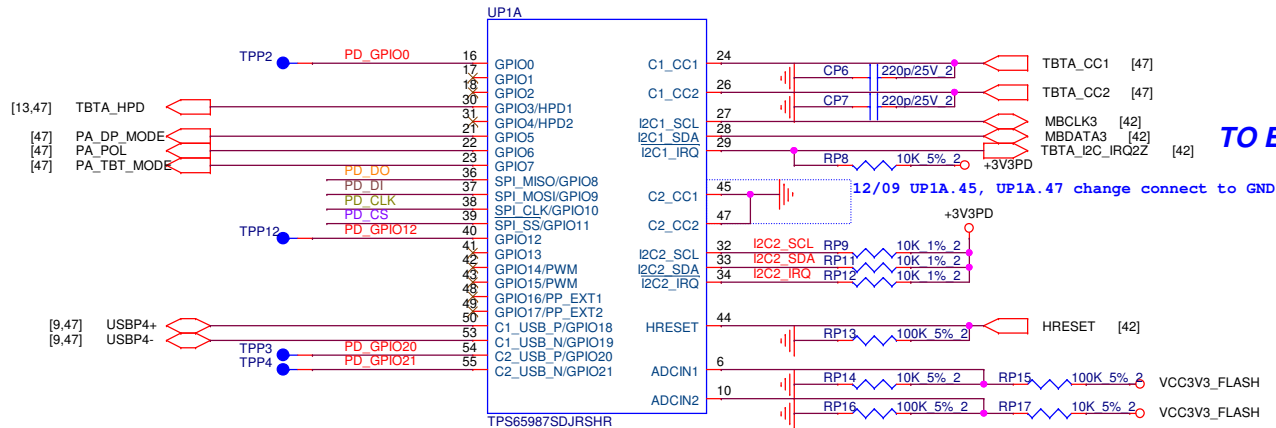
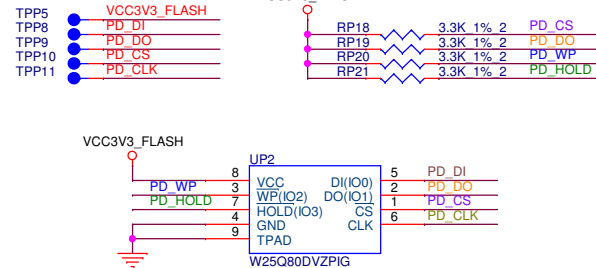
Size Custom	Document Number NA	Rev 1A
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PD TPS65987SDJRSHR




PD SPI ROM



10/08 UP1 change to AL180901000

Qunata PN	Part Description
AL180901000	IC OTHER(56P) SN1809018RSHR(VQFN)
AL180901003	IC OTHER(56P) SN1809018RSHR(VQFN)TOPBS



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Table 7. TUSB546-DCI Receiver Equalization GPIO Control

Equalization Setting #	USB3.1 DOWNSTREAM FACING PORTS			USB 3.1 UPSTREAM FACING PORT			ALL DISPLAYPORT Lanes		
	EQ1 PIN LEVEL	EQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN at 4.05 GHz (dB)
0	0	0	0.2	0	0	-1.6	0	0	1.0
1	0	R	1.2	0	R	-0.5	0	R	3.3
2	0	F	2.2	0	F	0.5	0	F	4.9
3	0	1	3.3	0	1	1.6	0	1	6.5
4	R	0	4.2	R	0	2.4	R	0	7.5
5	R	R	5.1	R	R	3.4	R	R	8.6
6	R	F	5.9	R	F	4.1	R	F	9.5
7	R	1	6.7	R	1	4.9	R	1	10.4
8	F	0	7.4	F	0	5.7	F	0	11.1
9	F	R	8.1	F	R	6.4	F	R	11.7
10	F	F	8.7	F	F	6.9	F	F	12.3
11	F	1	9.3	F	1	7.5	F	1	12.8
12	1	0	9.7	1	0	8.0	1	0	13.2
13	1	R	10.2	1	R	8.5	1	R	13.6
14	1	F	10.6	1	F	8.9	1	F	14.0
15	1	1	11.1	1	1	9.4	1	1	14.4

TUSB546 Pin Control Mode

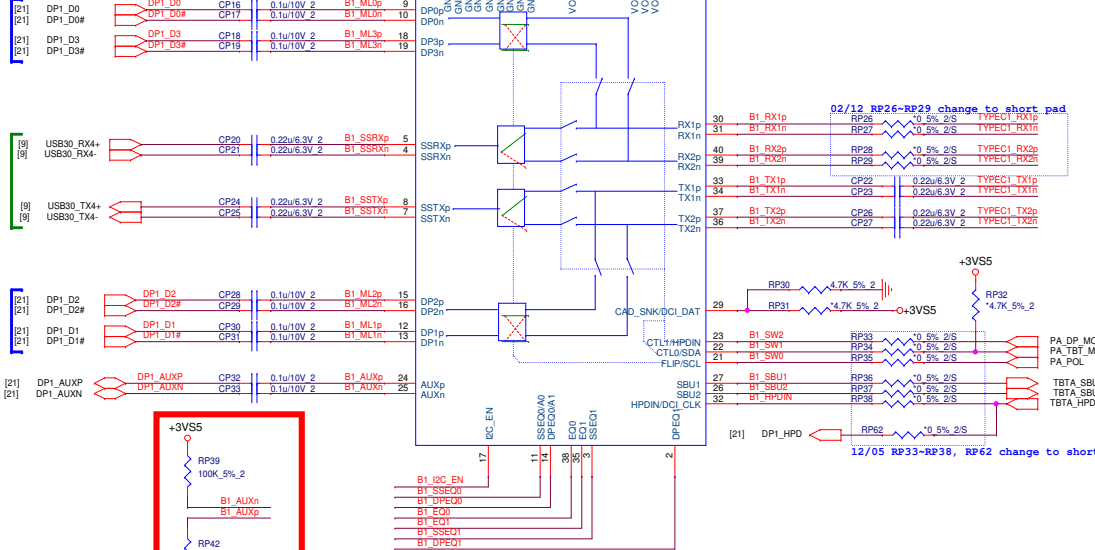
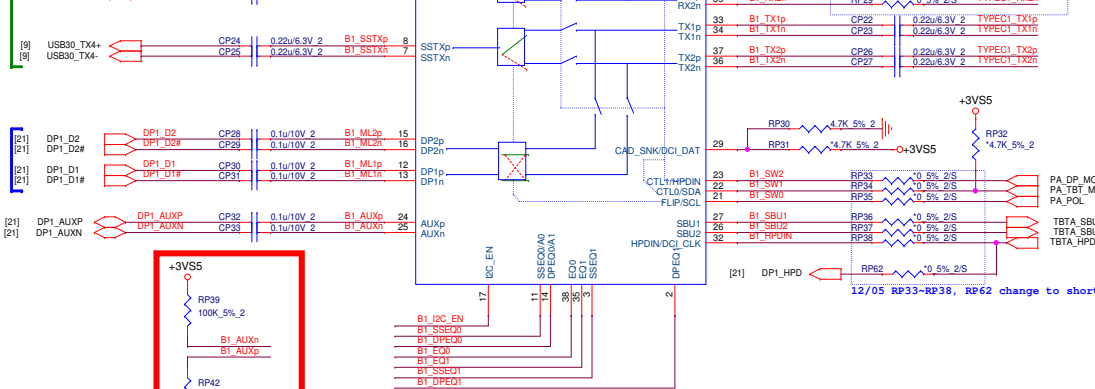
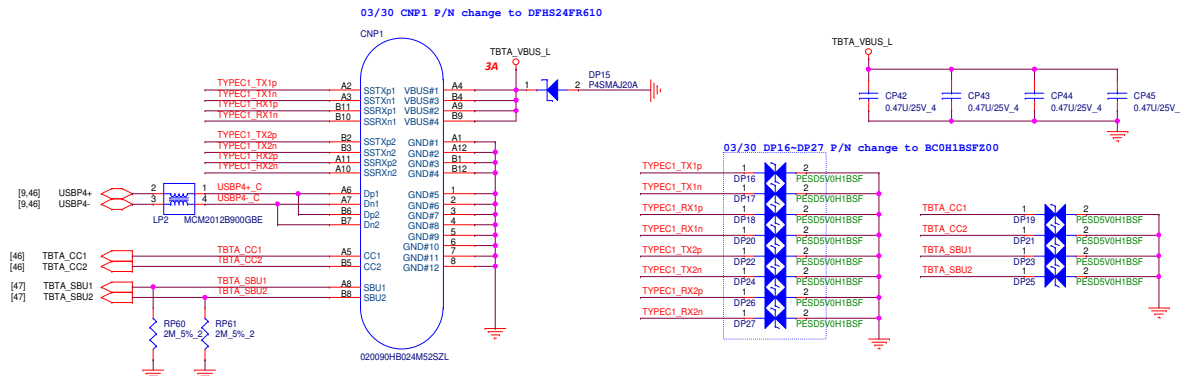
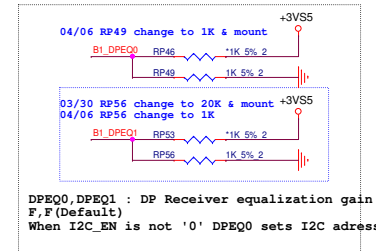
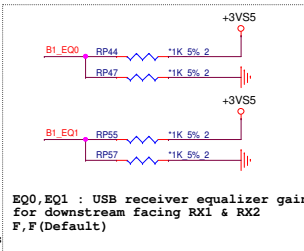
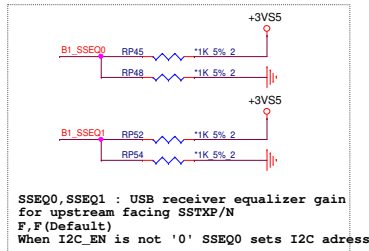
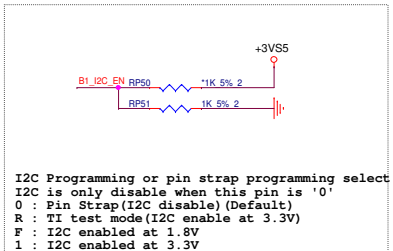
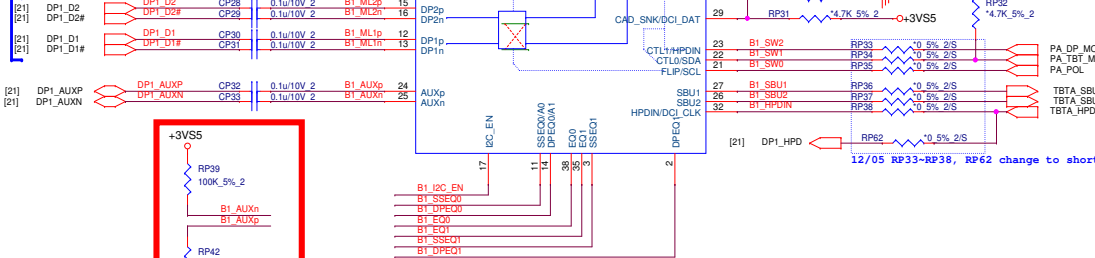
CTL1	FLIP	AUX Select	TUSB546 Mode Selection
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	One Port USB 3.1 - No Flip
L	H	H	One Port USB 3.1 - With Flip
H	L	L	4 Lane DP - No Flip
H	L	H	4 Lane DP - With Flip
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flip
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flip

AUX Pin Control Mode

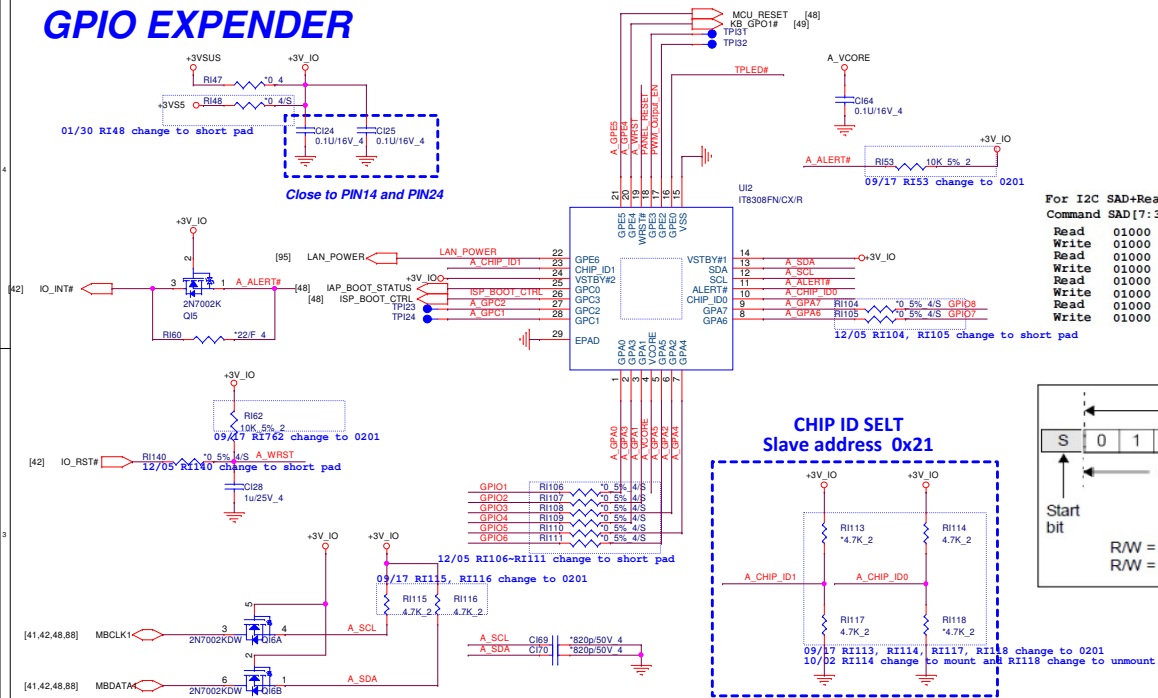
CTL1	FLIP	AUX Select
H	L	AUXP->SBU1, AUXN->SBU2
H	H	AUXP->SBU2, AUXN->SBU1
L	X	Open

4 Level Input:

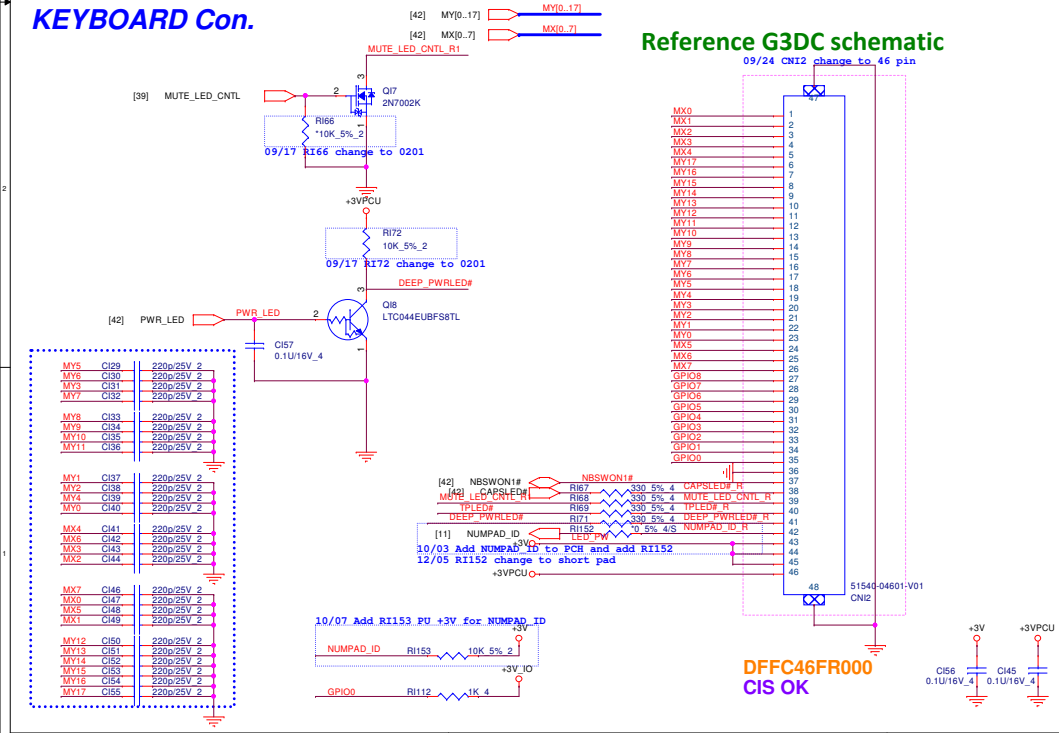
- L: Option1 Tie 1Kohm 5% to GND
- Option2 Directly tie to GND
- R: Tie 20kohm 5% to GND
- F: Float(leave pin open)
- 1: Option1 Tie 1Kohm 5% to Vcc
- Option2 Directly tie to Vcc

DisplayPort Source
From GPUUSB3.0 HOST
From PCHDisplayPort Source
From GPU

GPIO EXPENDER

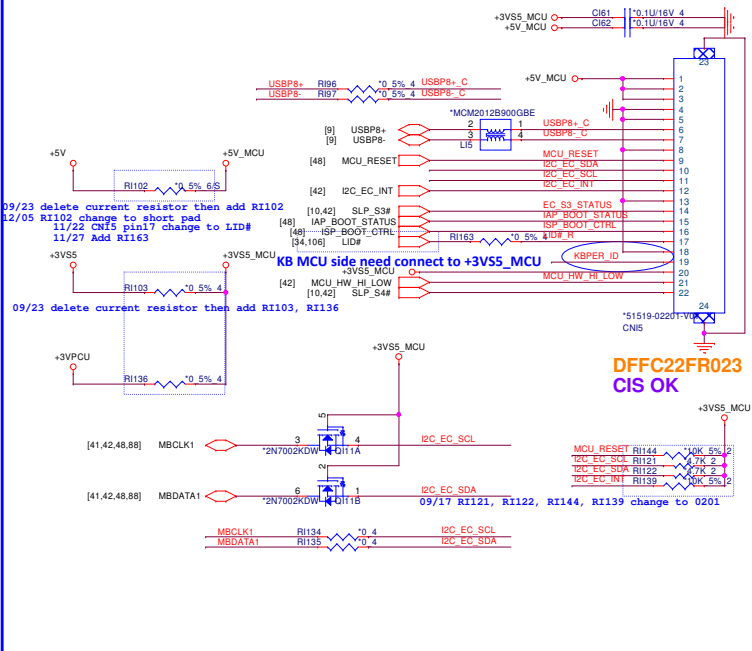


KEYBOARD Con.

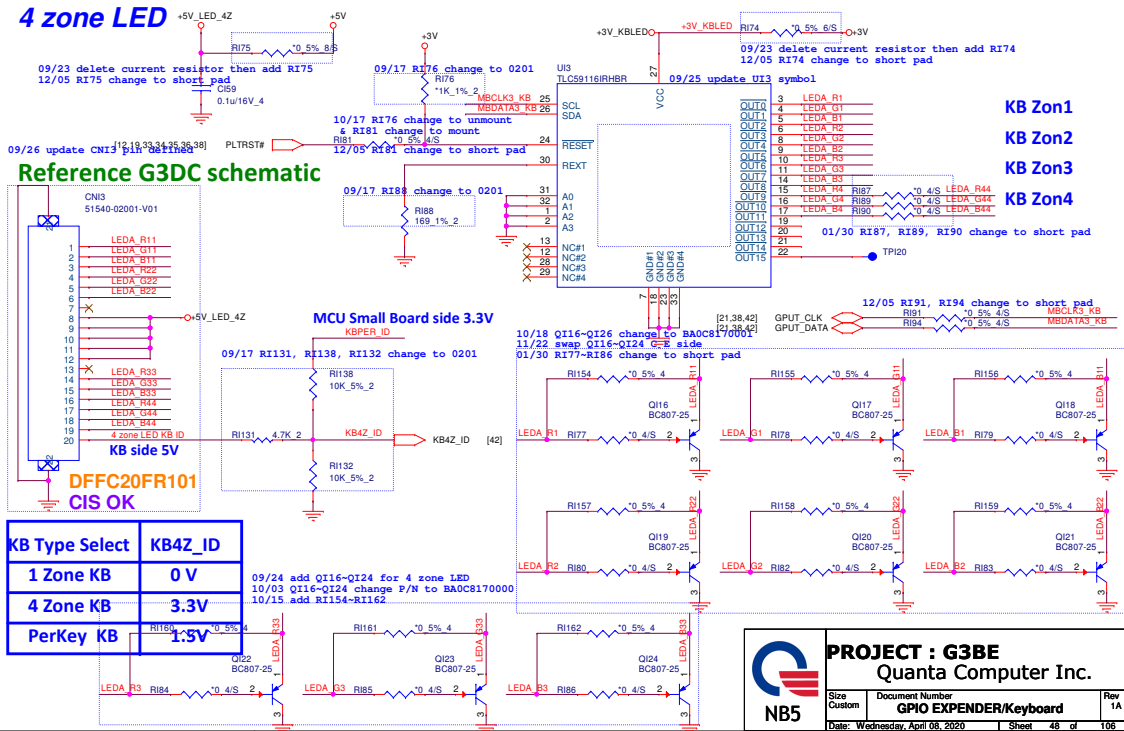


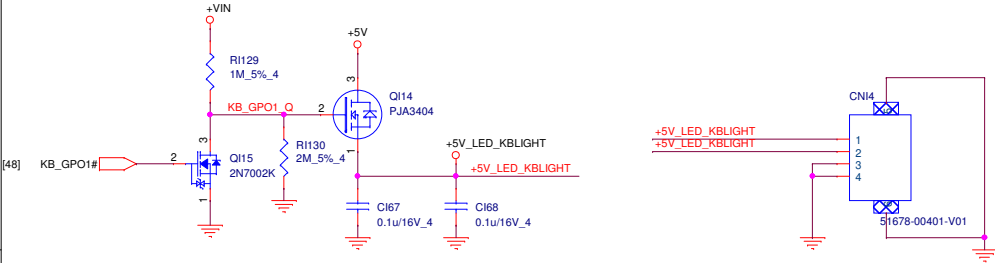
Per Key to MCU Board

01/21 Per Key parts change to unmount



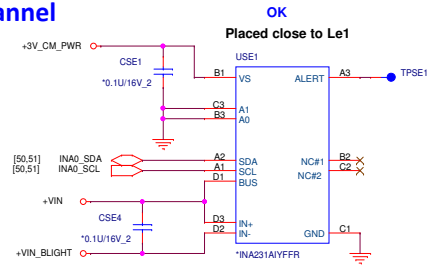
4 zone LED



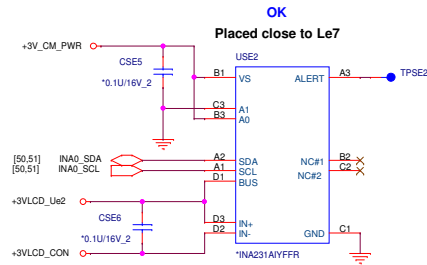


Panel-LCD Blight
Slave Addresses:1000000

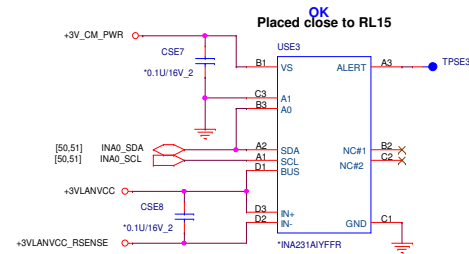
A0 Channel



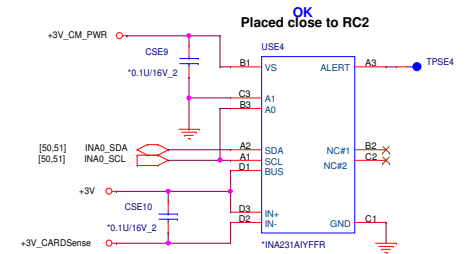
Panel-3V LCD Power
Slave Addresses:1000001



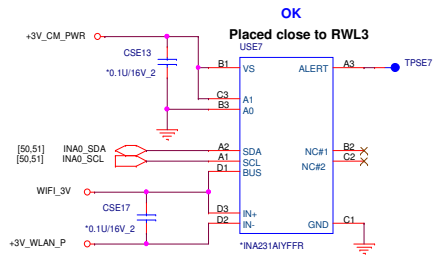
LAN
Slave Addresses:1000010



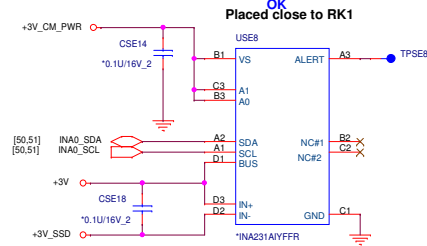
Card Reader
Slave Addresses:1000011



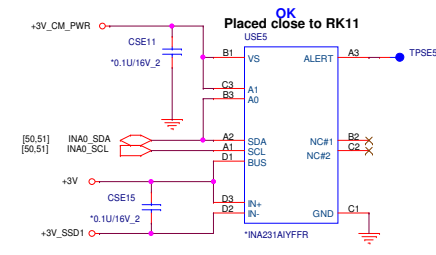
WLAN
Slave Addresses:1000100



SSD1
Slave Addresses:1000101



SSD2
Slave Addresses:1000110



FAN1
Slave Addresses:1000111

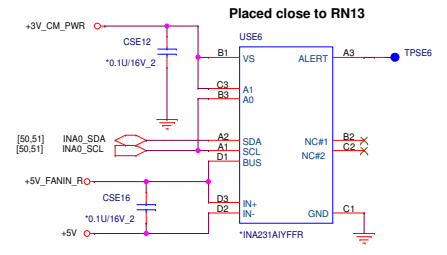
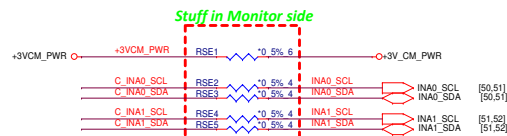
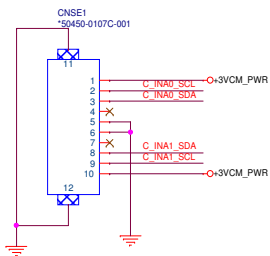
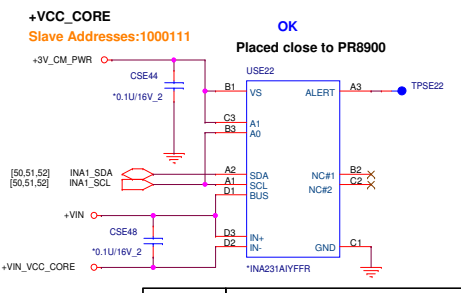
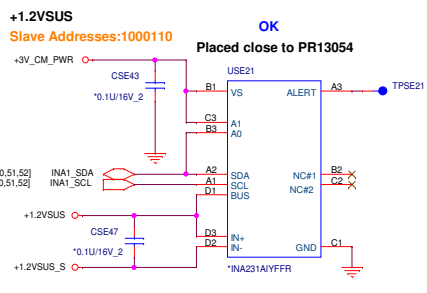
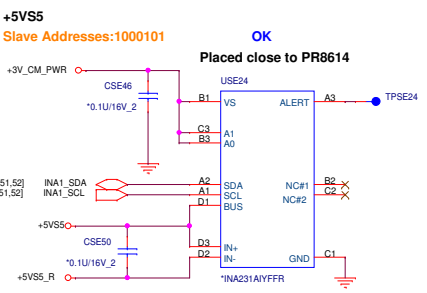
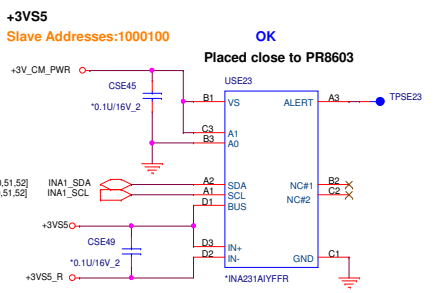
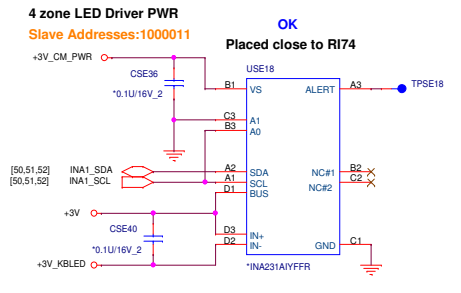
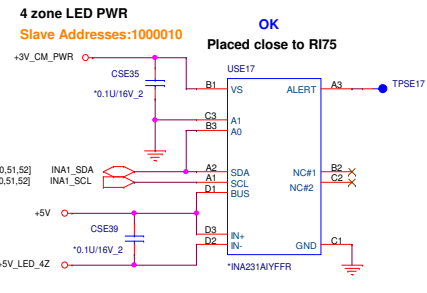
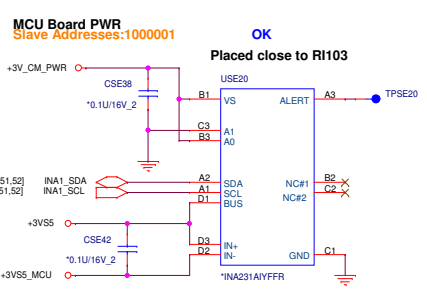
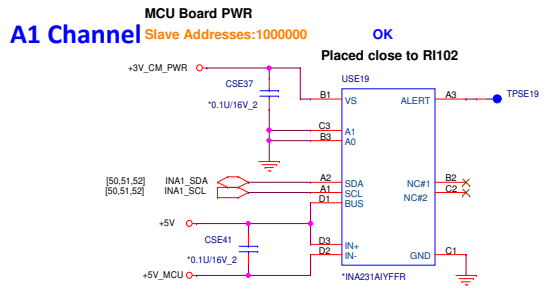
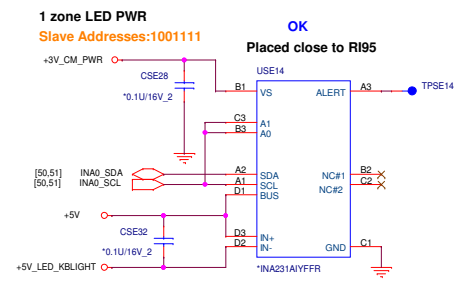
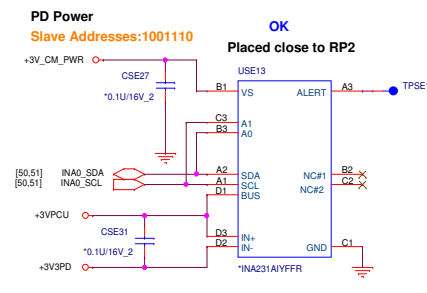
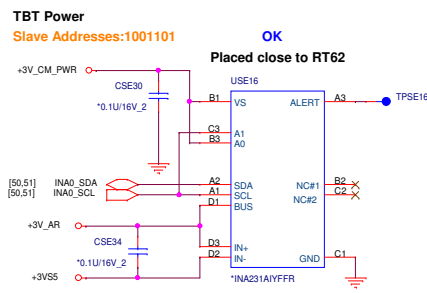
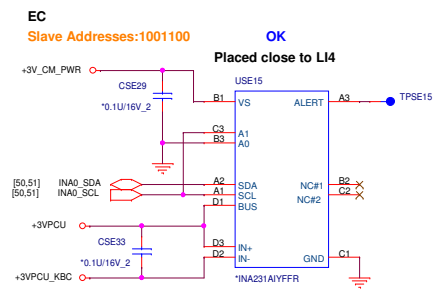
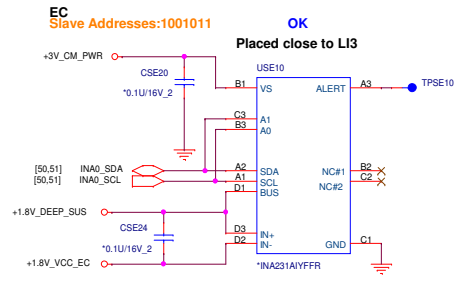
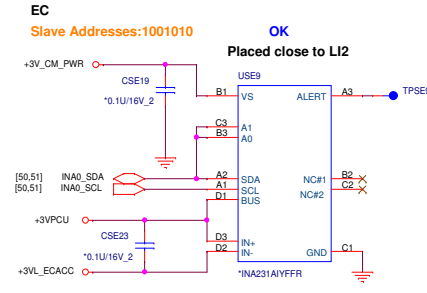
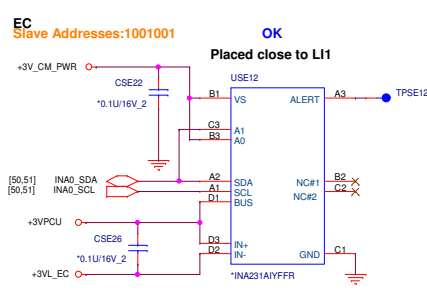
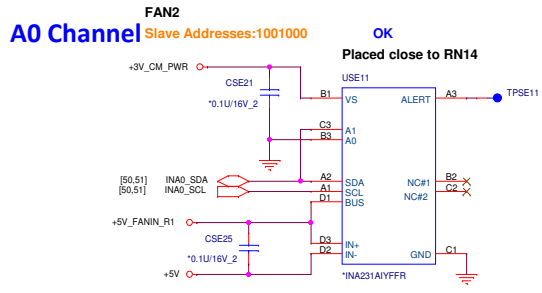
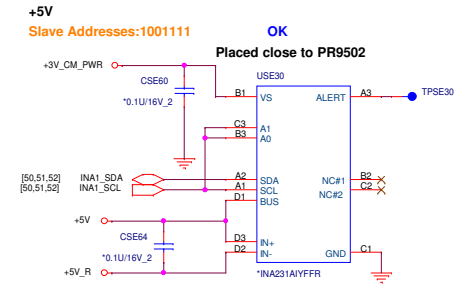
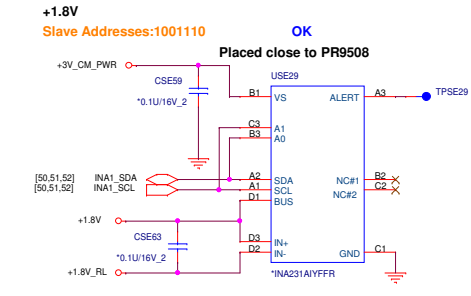
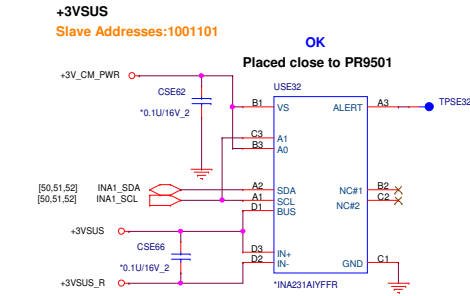
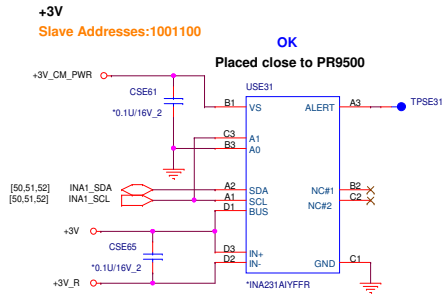
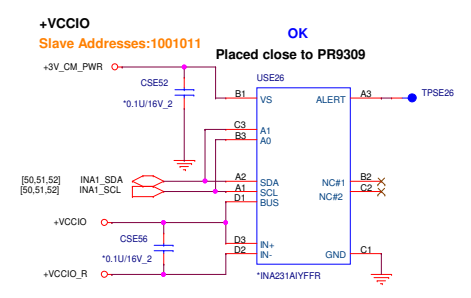
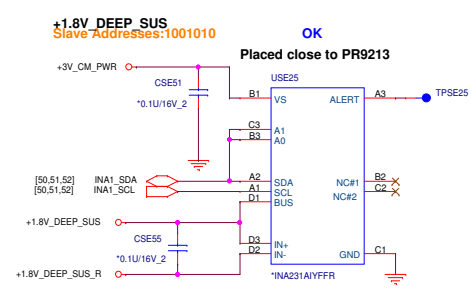
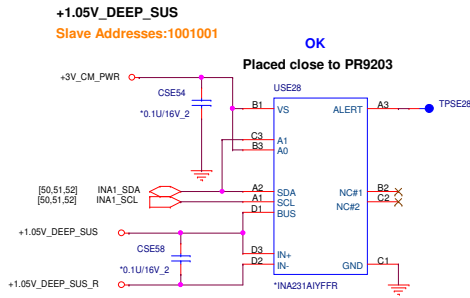
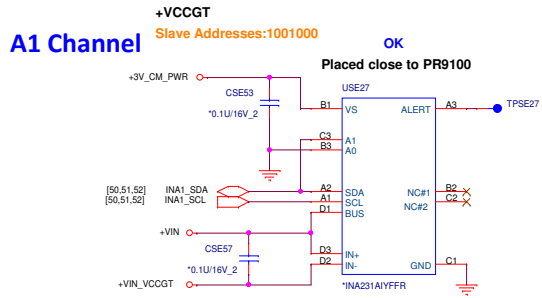


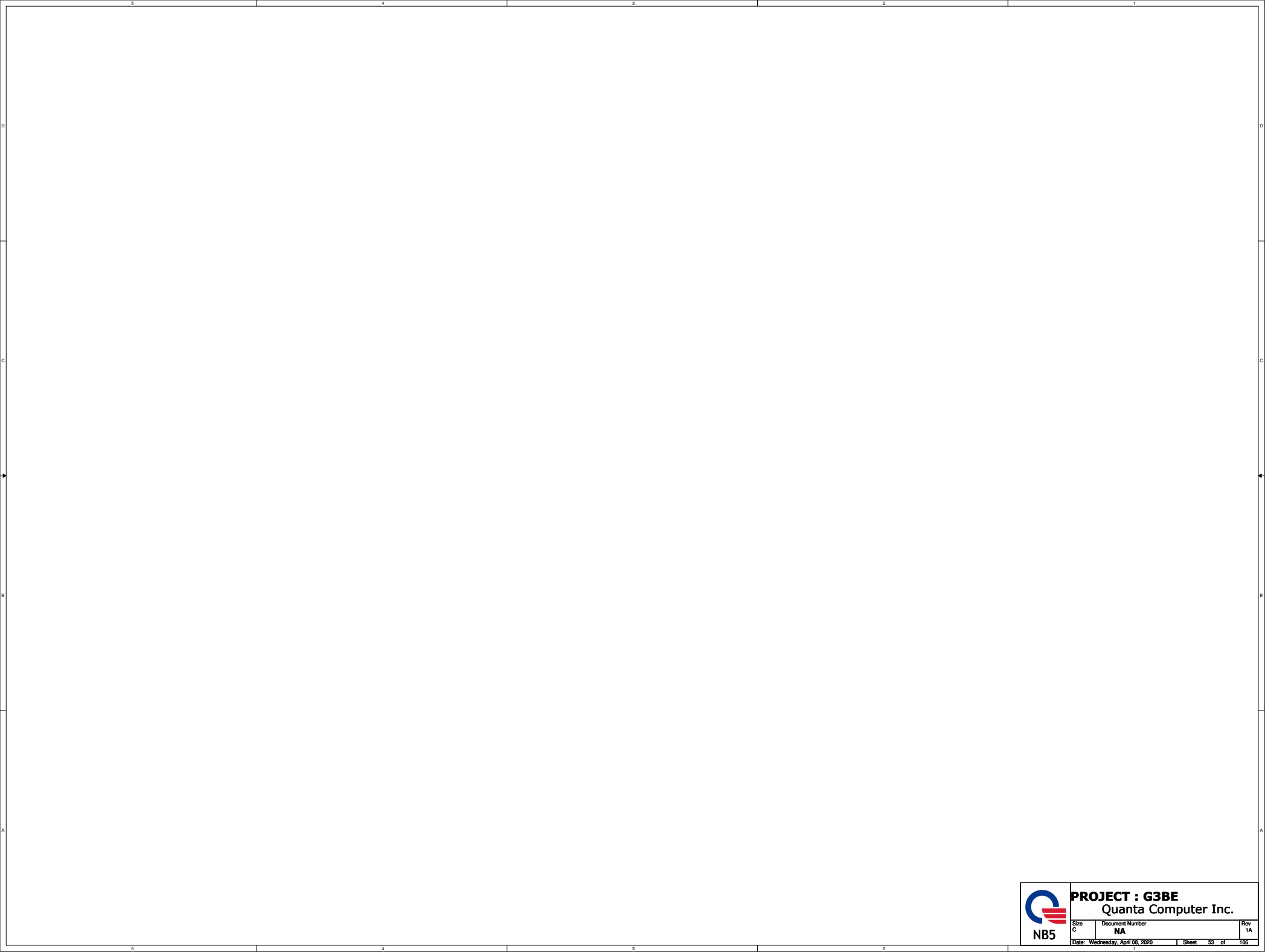
Table 7. INA231 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V _S	1000001
GND	SDA	1000010
GND	SCL	1000011
V _S	GND	1000100
V _S	V _S	1000101
V _S	SDA	1000110
V _S	SCL	1000111
SDA	GND	1001000
SDA	V _S	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V _S	1001101
SCL	SDA	1001110
SCL	SCL	1001111

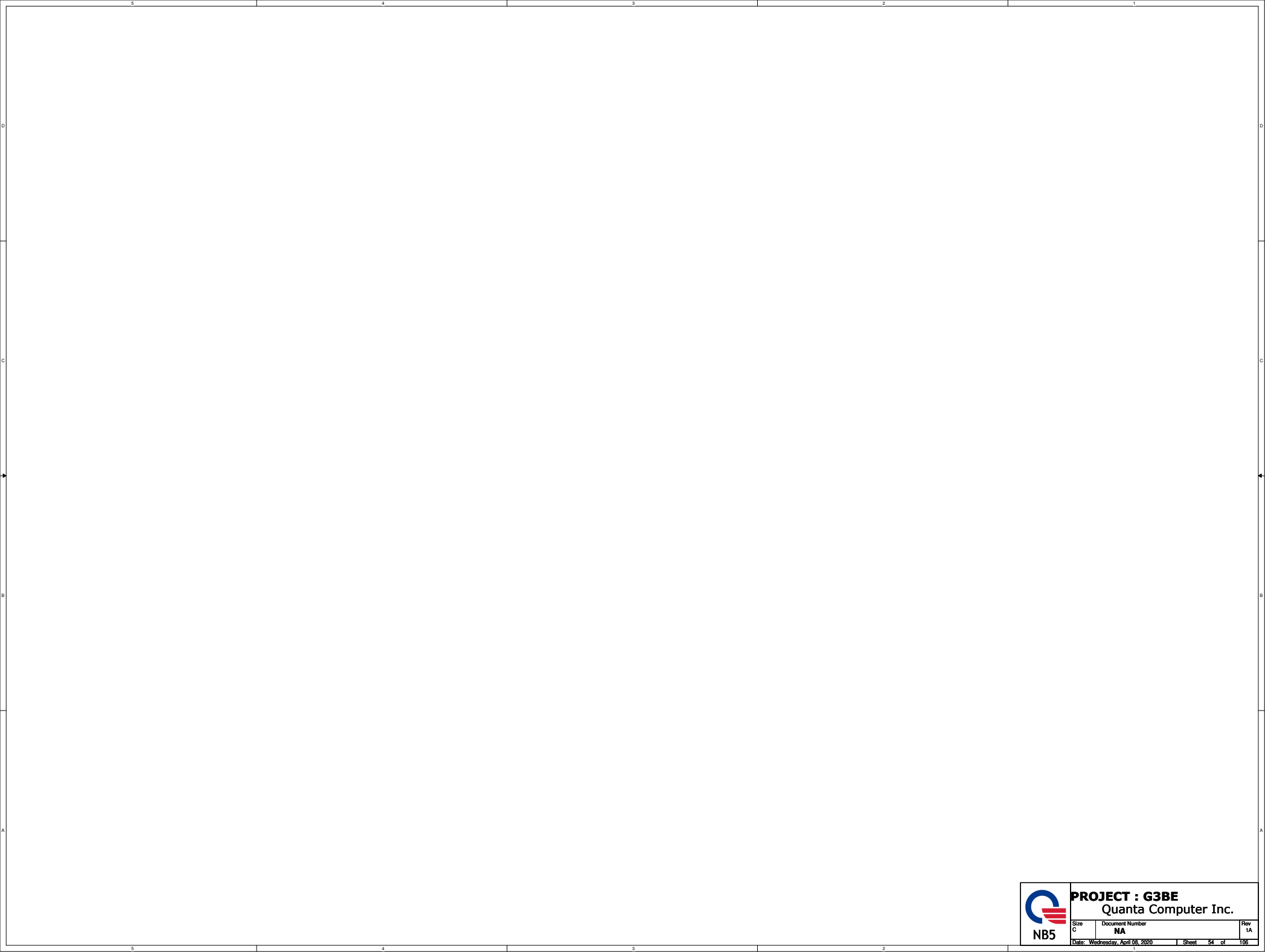









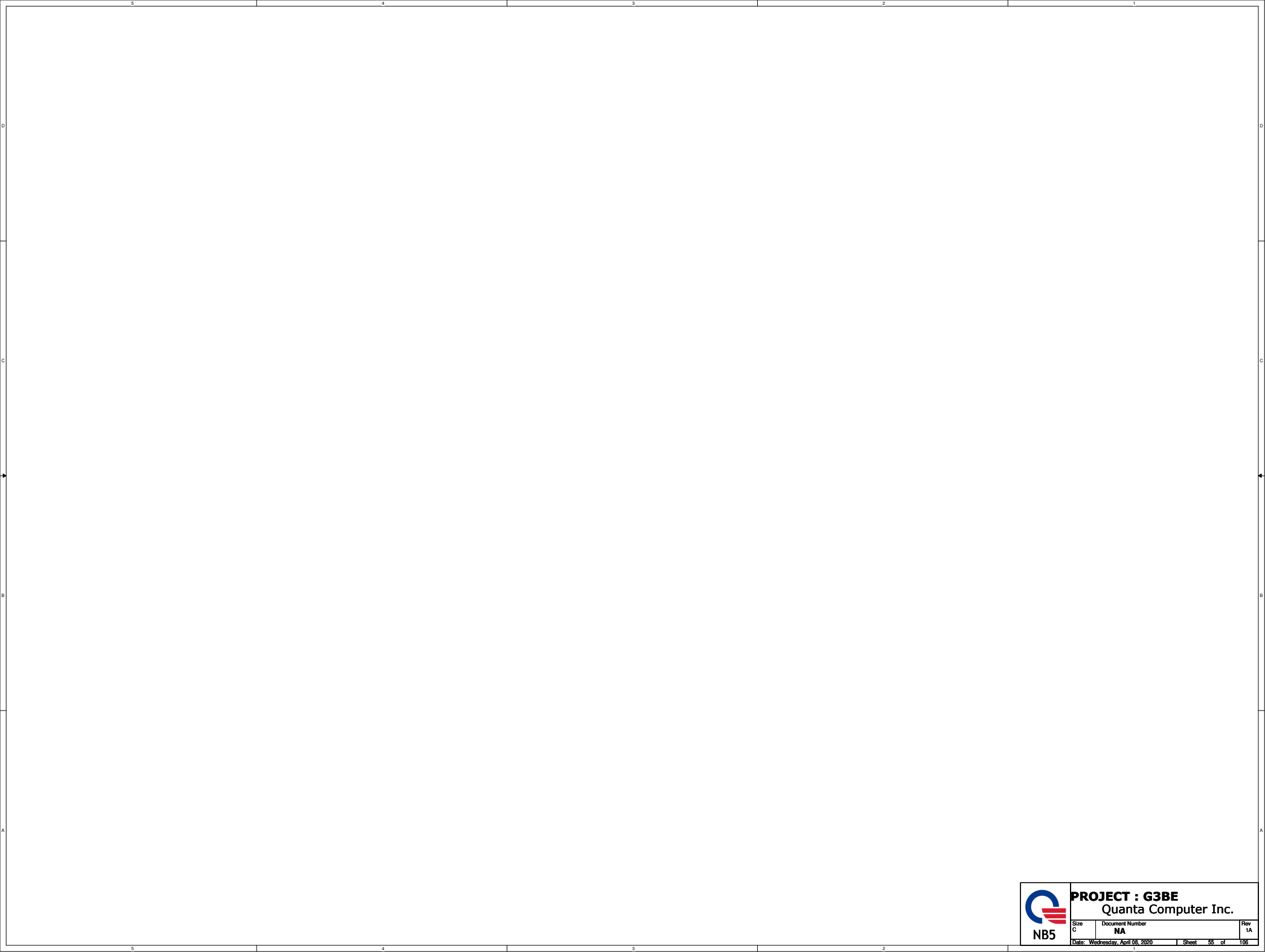
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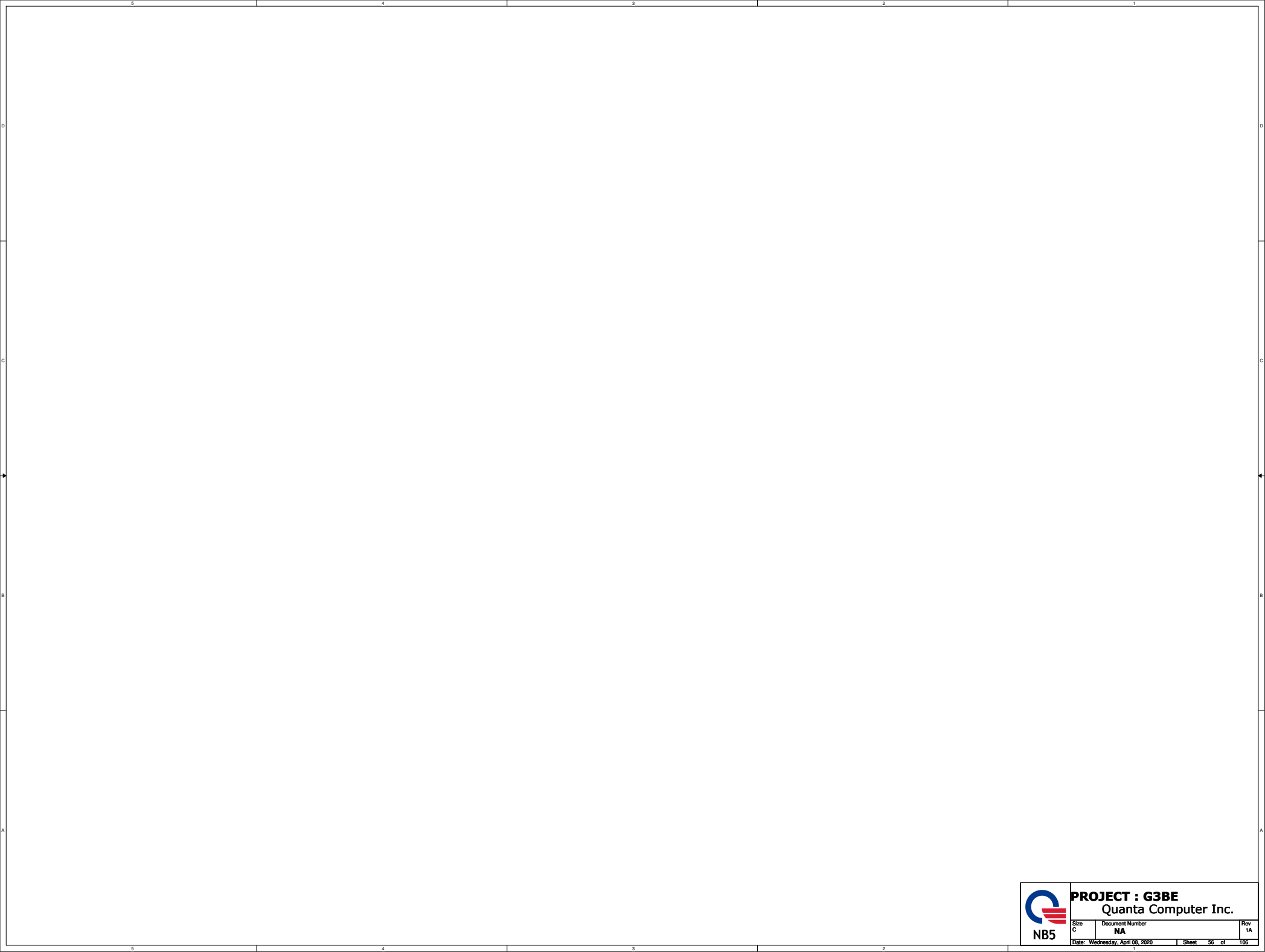


NB5


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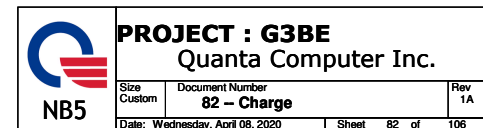
PROJECT : G3BE
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Quanta Computer Inc.


Size Custom	Document Number 81 – PWROK	Rev 1A
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Quanta Computer Inc.

Size Custom	Document Number 83 – Charger (ISL9538HRTZ-T)	Rev 1A
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Quanta Computer Inc.

Size Custom	Document Number 84 – Charge II	Rev 1A
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PROJECT : G3BE
Quanta Computer Inc.

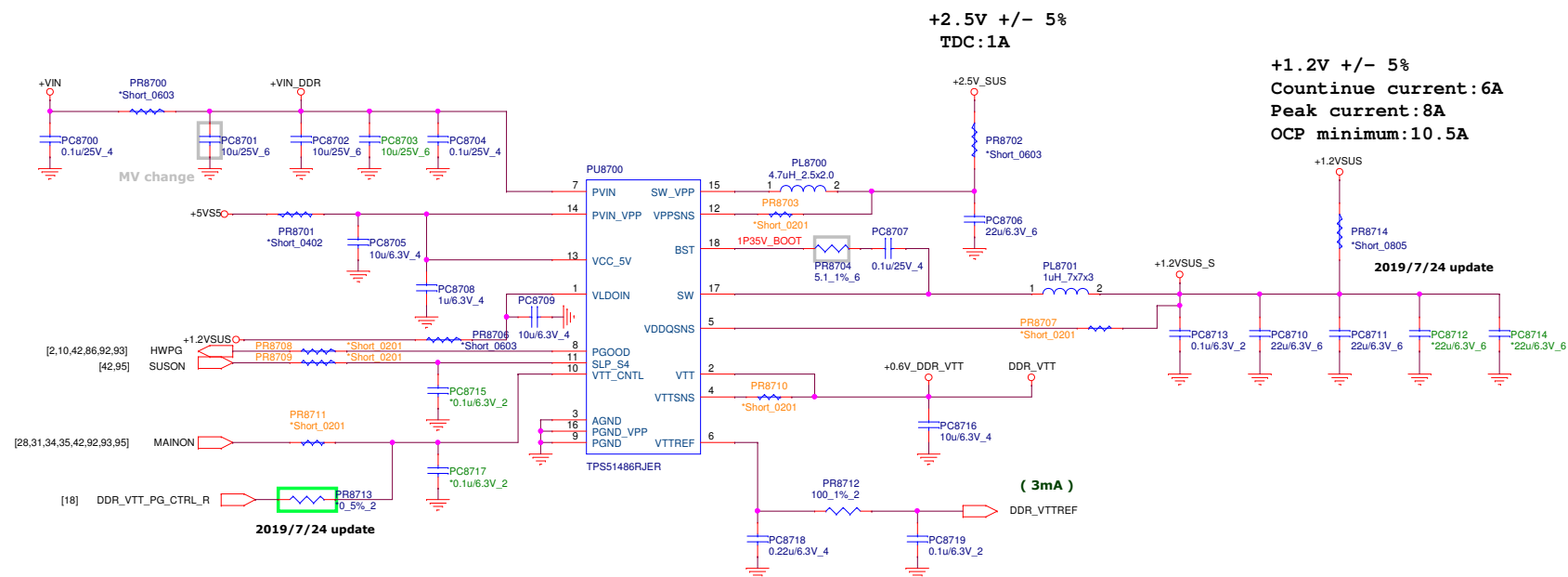
Size Custom	Document Number 85 – Charger II	Rev 1A
Date: Wednesday, April 08, 2020		Sheet 85 of 106

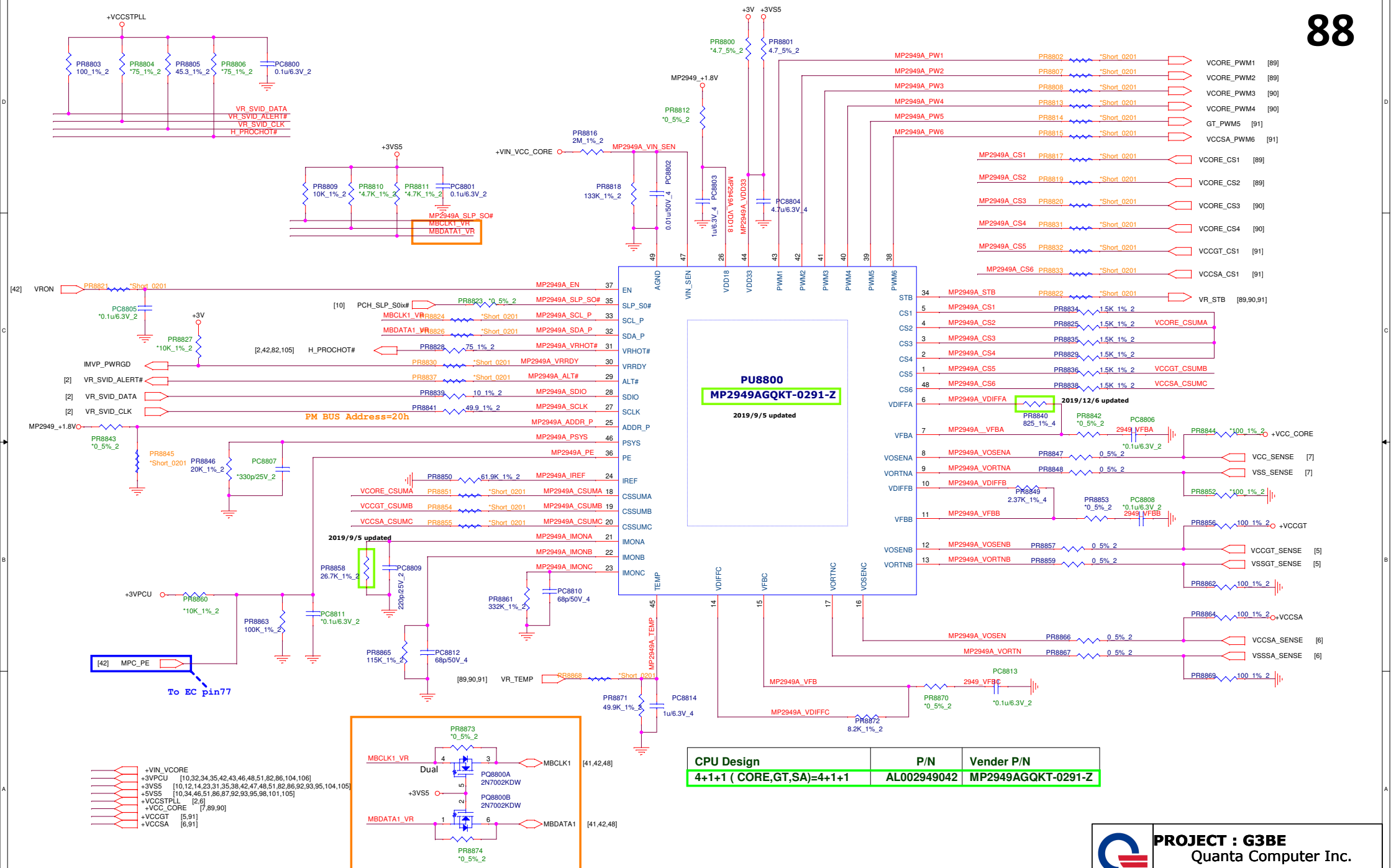
+3.3 Volt +/- 5%
EDP: 6A
EDP: 8A

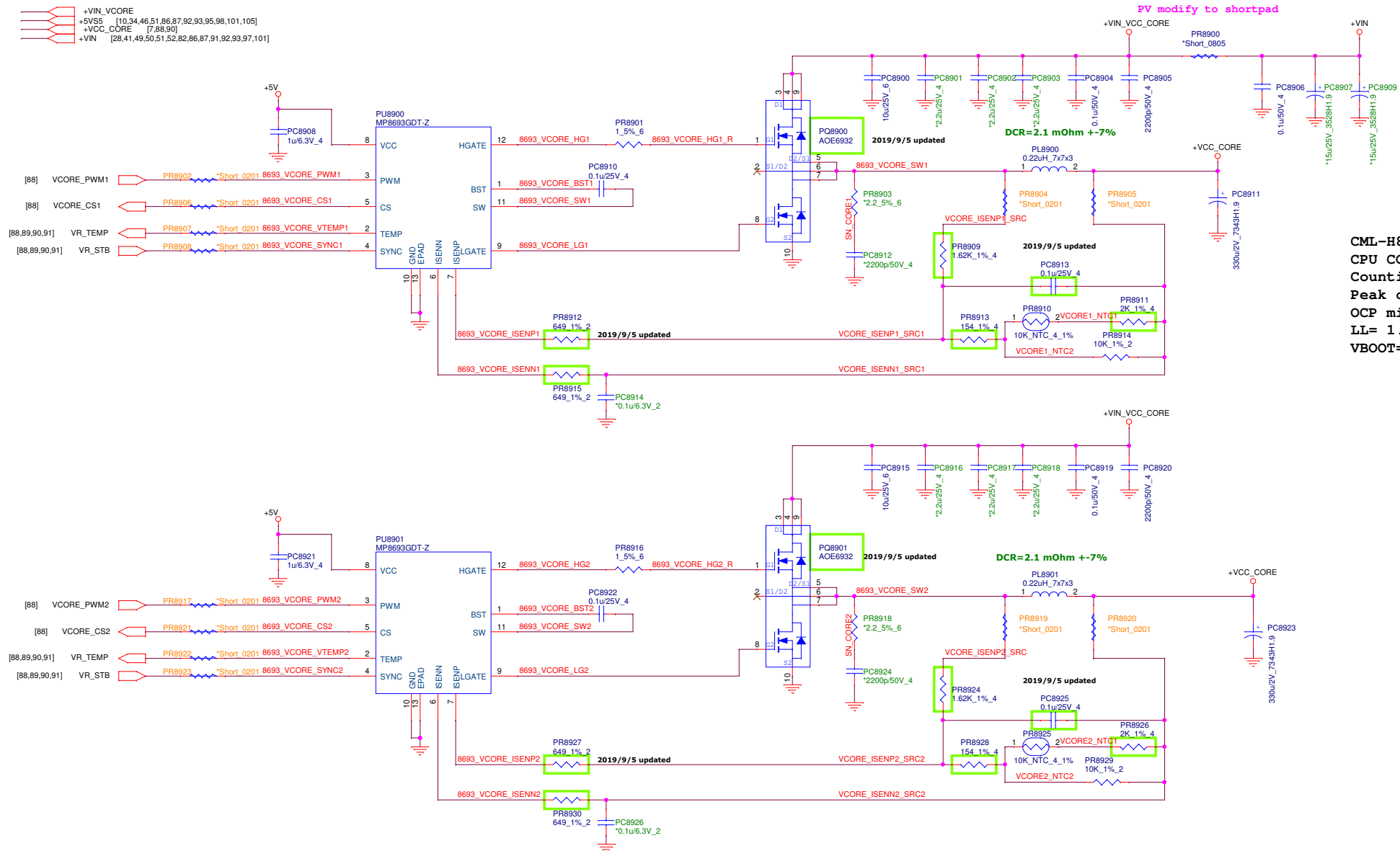


+5 Volt +/- 5%
TDC: 6A
EDP: 9A









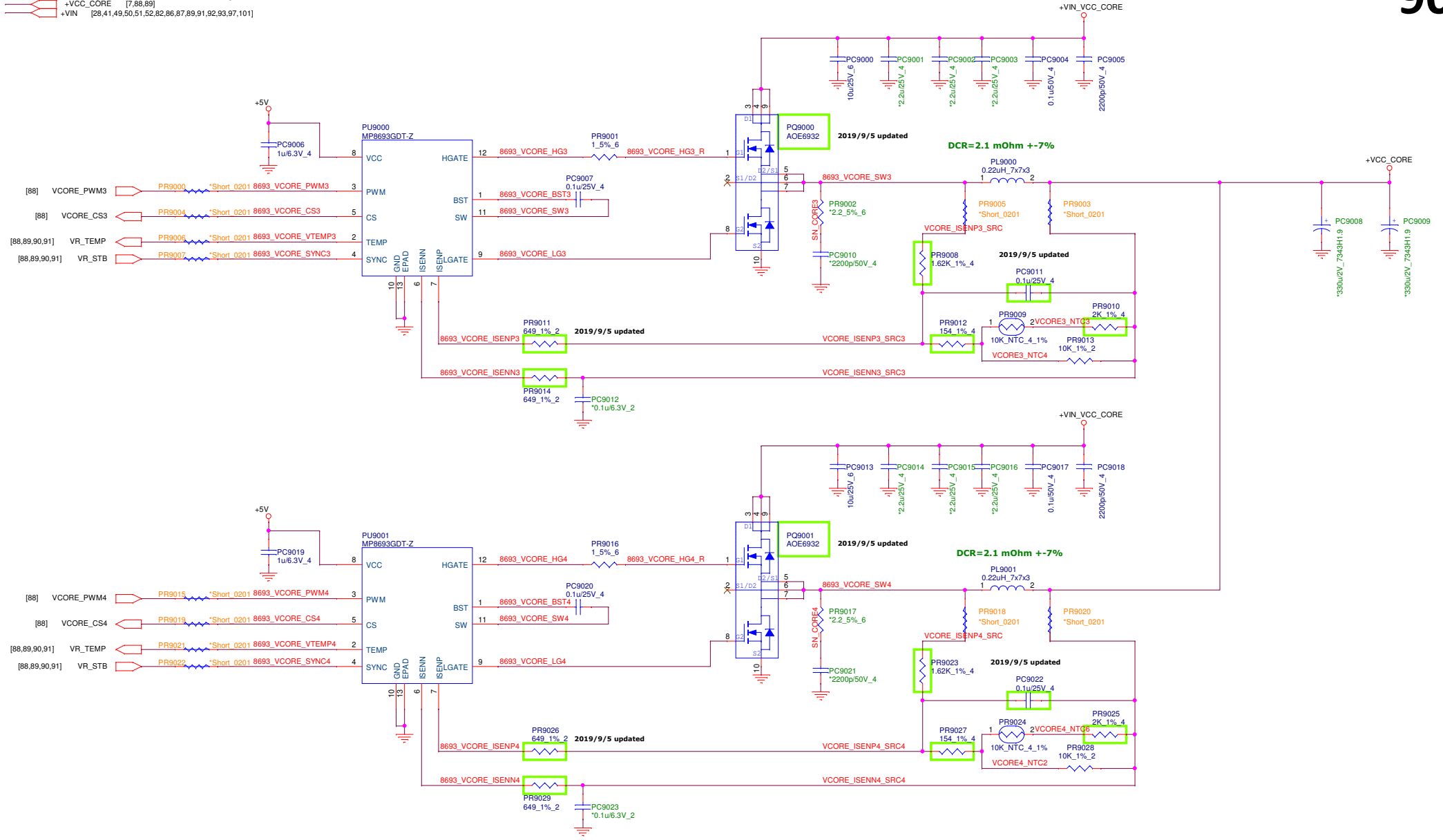
CML-H82 Baseline (35W)
CPU CORE Volt
Countinue current:86A
Peak current:140A
OCp minimum:168A
LL= 1.1mV/A
VBOOT=0V

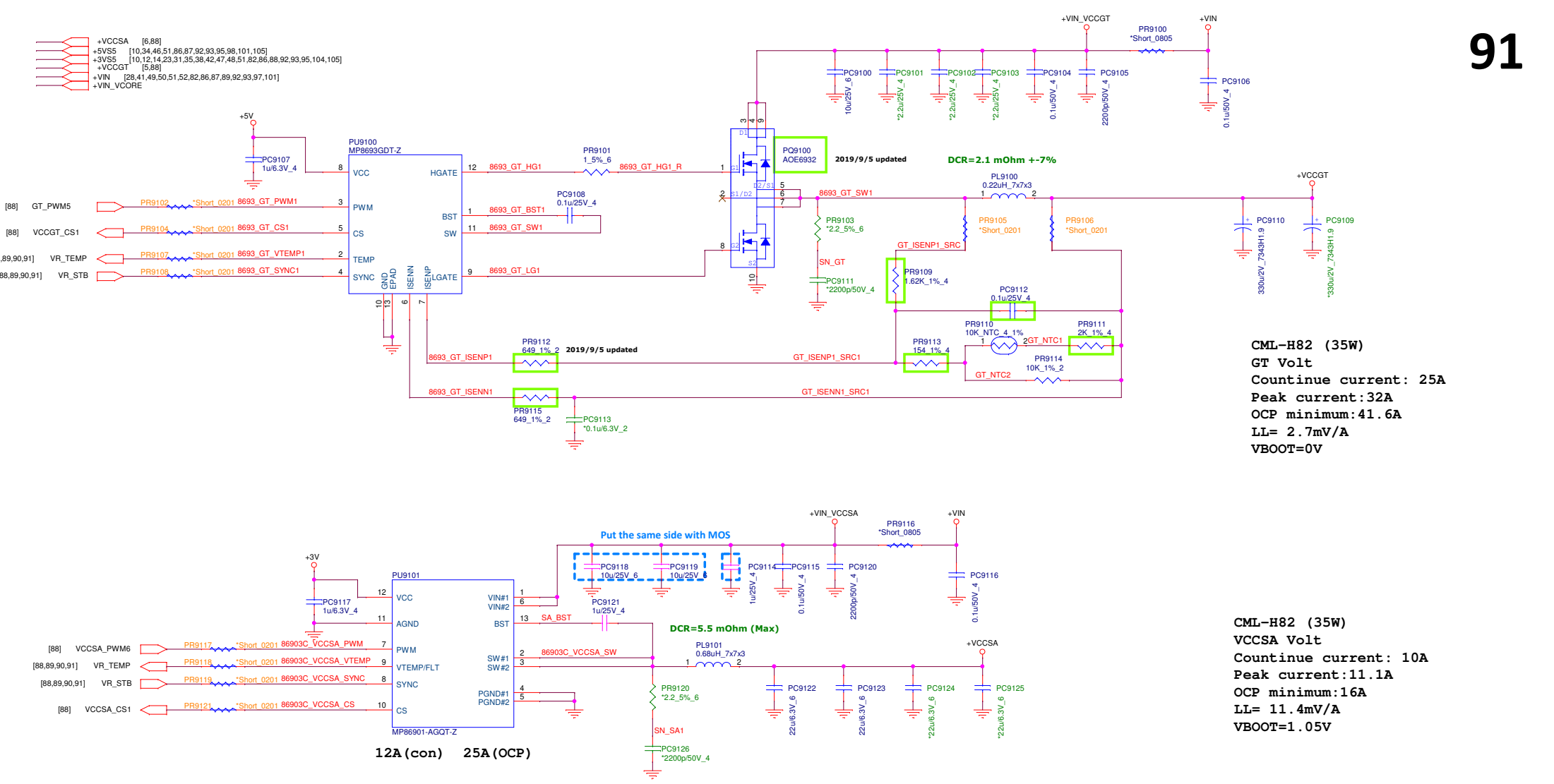


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Size Custom	Document Number 89 -- +VCC_CORE (MP86903-C)	Rev 1A
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+VIN_VCORE
+5VS5 [10,34,46,51,86,87,92,93,95,98,101,105]
+VCC_CORE [7,88,89]
+VIN [28,41,49,50,51,52,82,86,87,89,91,92,93,97,101]

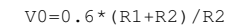
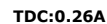


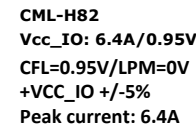


OCP minimum:12A

Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k




























EDP : 4A



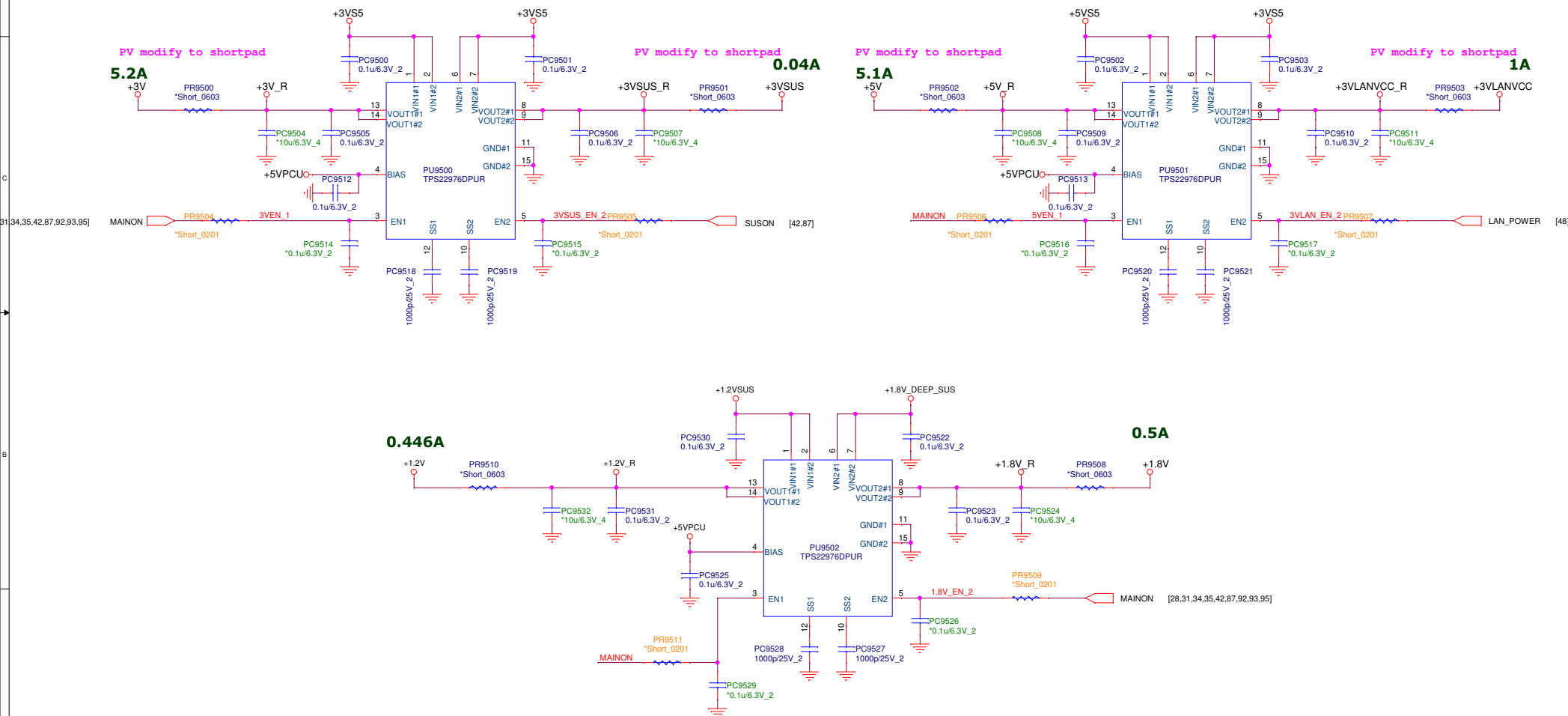



VID0_VCCIO	VID1_VCCIO	LP#	VCCIO
X	X	0	0V
0	0	1	0.85V
1	0	1	0.875V
0	1 (IC internal PU High)	1	0.95V

Default setting

-    +3V_DEEP_SUS [9,10,12,13,14,16,18]
   +VCCSTG [2,6,42]
   +3VS5 [10,12,14,23,31,35,38,42,47,48,51,82,86,88,92,95,104,105]
   +5VS5 [10,34,46,51,86,87,92,95,98,101,105]
   +VCCIO [3,6,52]
   +1.05V_DEEP_SUS [10,14,52,92]
   +1.2V_VCCPLL_OC [6]
   +1.2VSUS [2,6,10,17,18,51,87,95]
   +VIN [28,41,49,50,51,52,82,86,87,89,91,92,97,101]

+3V [9,10,11,13,16,17,18,21,28,30,31,33,34,36,38,39,41,42,48,50,51,52,82,88,91,98,99,101,105]
 +5VS5 [10,34,46,51,86,87,92,93,98,101,105]
 +3VS5 [10,12,14,23,31,35,38,42,47,48,51,82,86,88,92,93,104,105]
 +3VSUS [38,48,52]
 +5V [28,30,31,38,39,48,49,50,51,52,89,90,91,104]
 +3VLANVCC [33,50]
 +5VPCU [39,82,86,105]

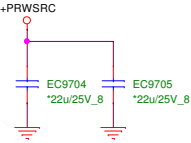
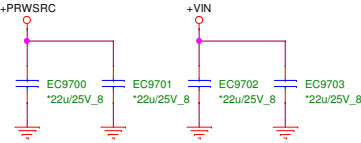


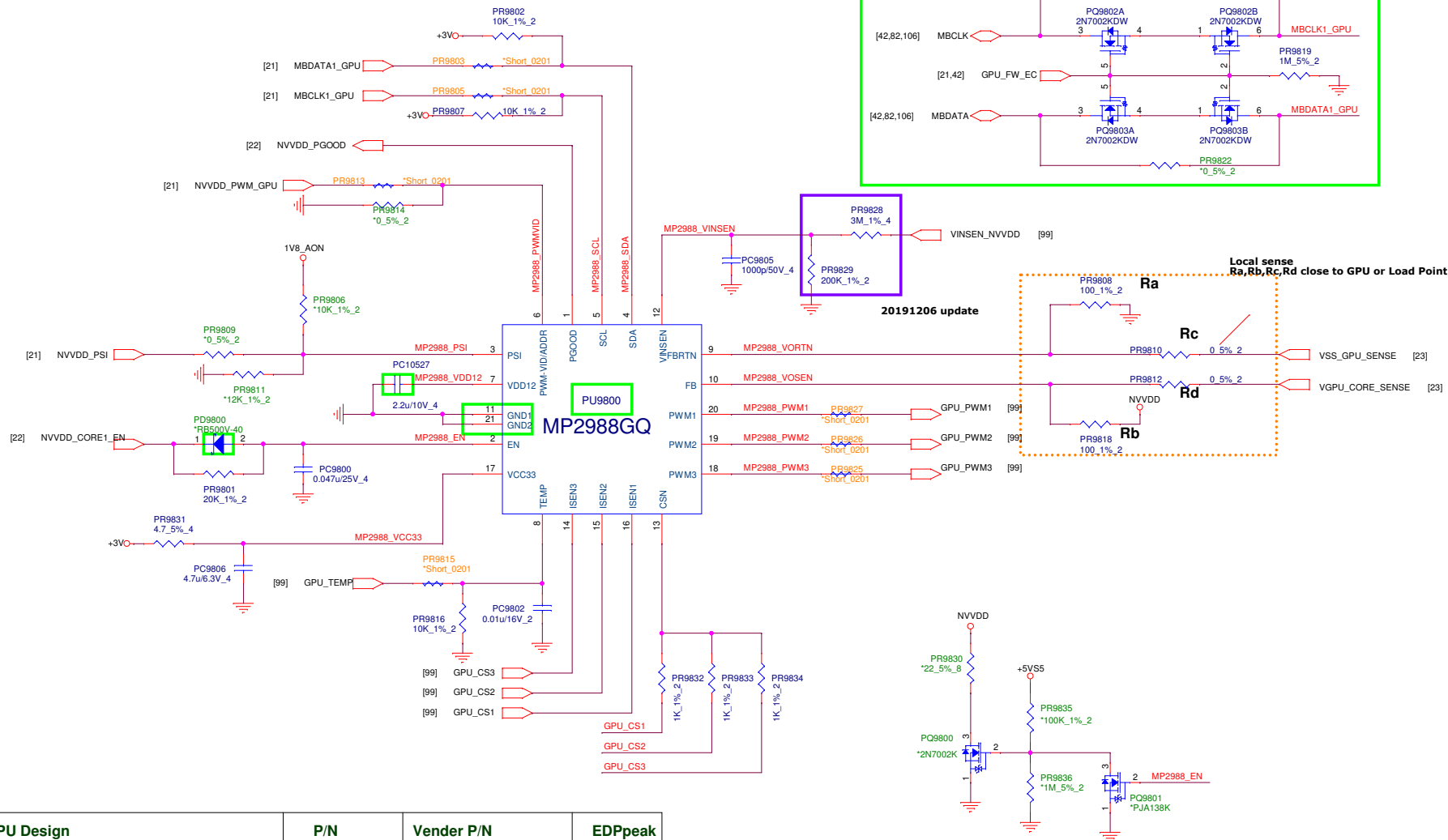


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Reserve for ISEN





GPU Design	P/N	Vender P/N	EDPpeak
3 Phase for N18P -G0 MAX P (50W/47A)		MP2988GQ-0060	109A
4 Phase for N17P-G1 (50W/59A)	AL002884003	MP2884AGU-0103-Z	106A
5 Phase for N18E -G0 MAXQ (60W/63A)	AL002886005	MP2886AGU-0125-Z	225A
6 Phase for N18E -G3 (80W/84A)	AL002886000	MP2886AGU-0112-Z	300A

Default setting

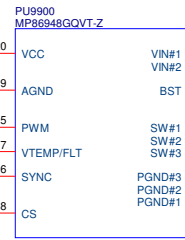
+VIN_GPU_TOTAL [101]
+5VS5 [10,34,46,51,86,87,92,93,95,98,101,105]
NVVDD [22,23,98]
+VIN_VGACORE

MOS Temperature

[98] GPU_PWM1
[98,99] GPU_TEMP
+3V
[98] GPU_CS1

PC9906
2.2u/10V_4

[98] VINSEN_NVVDD



Put the same side with Dr.MOS and near pin1

PR9900 *Short_0201

PC9900 PC9901 PC9902 PC9903 PC9904

10u/25V_5 10u/25V_6 10u/25V_7 1u/25V_4 2200p/50V_4

PC9905 *15u/25V_3528H1.9

PC9906 *15u/25V_7343H1.2

PC9907 *15u/25V_7343H1.2

PC9908 *15u/25V_7343H1.2

PC9909 *15u/25V_7343H1.2

PC9910 *15u/25V_7343H1.2

PC9911 *15u/25V_7343H1.2

PC9912 *15u/25V_7343H1.2

PC9913 *15u/25V_7343H1.2

PC9914 *15u/25V_7343H1.2

PC9915 *15u/25V_7343H1.2

PC9916 *15u/25V_7343H1.2

PC9917 *15u/25V_7343H1.2

PC9918 *15u/25V_7343H1.2

PC9919 *15u/25V_7343H1.2

PC9920 *15u/25V_7343H1.2

PC9921 *15u/25V_7343H1.2

PC9922 *15u/25V_7343H1.2

PC9923 *15u/25V_7343H1.2

PC9924 *15u/25V_7343H1.2

PC9925 *15u/25V_7343H1.2

PC9926 *15u/25V_7343H1.2

PC9927 *15u/25V_7343H1.2

PC9928 *15u/25V_7343H1.2

PC9929 *15u/25V_7343H1.2

PC9930 *15u/25V_7343H1.2

PC9931 *15u/25V_7343H1.2

PC9932 *15u/25V_7343H1.2

PC9933 *15u/25V_7343H1.2

PC9934 *15u/25V_7343H1.2

PC9935 *15u/25V_7343H1.2

PC9936 *15u/25V_7343H1.2

PC9937 *15u/25V_7343H1.2

PC9938 *15u/25V_7343H1.2

PC9939 *15u/25V_7343H1.2

PC9940 *15u/25V_7343H1.2

PC9941 *15u/25V_7343H1.2

PC9942 *15u/25V_7343H1.2

PC9943 *15u/25V_7343H1.2

PC9944 *15u/25V_7343H1.2

PC9945 *15u/25V_7343H1.2

PC9946 *15u/25V_7343H1.2

PC9947 *15u/25V_7343H1.2

PC9948 *15u/25V_7343H1.2

PC9949 *15u/25V_7343H1.2

PC9950 *15u/25V_7343H1.2

PC9951 *15u/25V_7343H1.2

PC9952 *15u/25V_7343H1.2

PC9953 *15u/25V_7343H1.2

PC9954 *15u/25V_7343H1.2

PC9955 *15u/25V_7343H1.2

PC9956 *15u/25V_7343H1.2

PC9957 *15u/25V_7343H1.2

PC9958 *15u/25V_7343H1.2

PC9959 *15u/25V_7343H1.2

PC9960 *15u/25V_7343H1.2

PC9961 *15u/25V_7343H1.2

PC9962 *15u/25V_7343H1.2

PC9963 *15u/25V_7343H1.2

PC9964 *15u/25V_7343H1.2

PC9965 *15u/25V_7343H1.2

PC9966 *15u/25V_7343H1.2

PC9967 *15u/25V_7343H1.2

PC9968 *15u/25V_7343H1.2

PC9969 *15u/25V_7343H1.2

PC9970 *15u/25V_7343H1.2

PC9971 *15u/25V_7343H1.2

PC9972 *15u/25V_7343H1.2

PC9973 *15u/25V_7343H1.2

PC9974 *15u/25V_7343H1.2

PC9975 *15u/25V_7343H1.2

PC9976 *15u/25V_7343H1.2

PC9977 *15u/25V_7343H1.2

PC9978 *15u/25V_7343H1.2

PC9979 *15u/25V_7343H1.2

PC9980 *15u/25V_7343H1.2

PC9981 *15u/25V_7343H1.2

PC9982 *15u/25V_7343H1.2

PC9983 *15u/25V_7343H1.2

PC9984 *15u/25V_7343H1.2

PC9985 *15u/25V_7343H1.2

PC9986 *15u/25V_7343H1.2

PC9987 *15u/25V_7343H1.2

PC9988 *15u/25V_7343H1.2

PC9989 *15u/25V_7343H1.2

PC9990 *15u/25V_7343H1.2

PC9991 *15u/25V_7343H1.2

PC9992 *15u/25V_7343H1.2

PC9993 *15u/25V_7343H1.2

PC9994 *15u/25V_7343H1.2

PC9995 *15u/25V_7343H1.2

PC9996 *15u/25V_7343H1.2

PC9997 *15u/25V_7343H1.2

PC9998 *15u/25V_7343H1.2

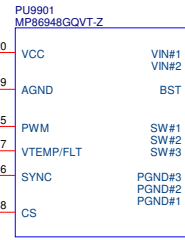
PC9999 *15u/25V_7343H1.2

PC10000 *15u/25V_7343H1.2

N18P G0 MP
GPU CORE Volt
Continue current:47A
Peak current: 109A/6uSec.
OCP Minimum: 130A.
LL=
VBOOT=0.8V
Eff > 86%
DC < +/- 20mV
Setting time <100uS

PC9914
2.2u/10V_4

[98] VINSEN_NVVDD



Put the same side with Dr.MOS and near pin1

PR9905 *Short_0201

PC9915 PC9916 PC9917 PC9918 PC9919

10u/25V_5 10u/25V_6 10u/25V_7 1u/25V_4 2200p/50V_4

PC9920 *15u/25V_3528H1.9

PC9921 *15u/25V_7343H1.2

PC9922 *15u/25V_7343H1.2

PC9923 *15u/25V_7343H1.2

PC9924 *15u/25V_7343H1.2

PC9925 *15u/25V_7343H1.2

PC9926 *15u/25V_7343H1.2

PC9927 *15u/25V_7343H1.2

PC9928 *15u/25V_7343H1.2

PC9929 *15u/25V_7343H1.2

PC9930 *15u/25V_7343H1.2

PC9931 *15u/25V_7343H1.2

PC9932 *15u/25V_7343H1.2

PC9933 *15u/25V_7343H1.2

PC9934 *15u/25V_7343H1.2

PC9935 *15u/25V_7343H1.2

PC9936 *15u/25V_7343H1.2

PC9937 *15u/25V_7343H1.2

PC9938 *15u/25V_7343H1.2

PC9939 *15u/25V_7343H1.2

PC9940 *15u/25V_7343H1.2

PC9941 *15u/25V_7343H1.2

PC9942 *15u/25V_7343H1.2

PC9943 *15u/25V_7343H1.2

PC9944 *15u/25V_7343H1.2

PC9945 *15u/25V_7343H1.2

PC9946 *15u/25V_7343H1.2

PC9947 *15u/25V_7343H1.2

PC9948 *15u/25V_7343H1.2

PC9949 *15u/25V_7343H1.2

PC9950 *15u/25V_7343H1.2

PC9951 *15u/25V_7343H1.2

PC9952 *15u/25V_7343H1.2

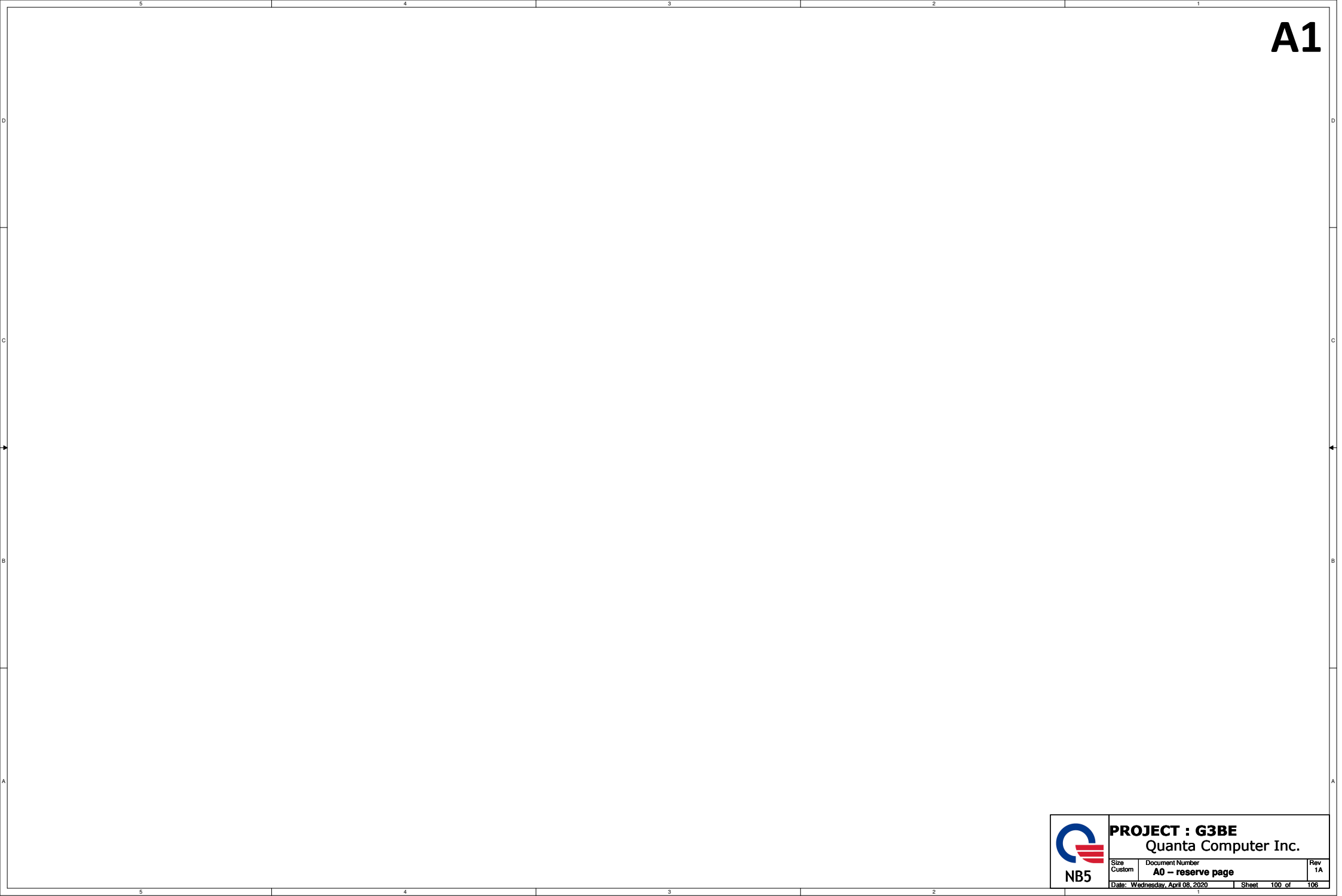
PC9953 *15u/25V_7343H1.2


PC9954 *15u/25V_7343H1.2

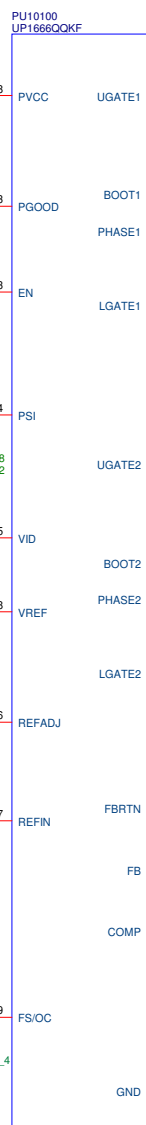
PC9955 *15u/25V_7343H1.2

PC9956 *15u/25V_7343H1.2

PC9957 *15u/25V_7343H1.2



 NB5	PROJECT : G3BE Quanta Computer Inc.		
	Size Custom	Document Number A0 – reserve page	Rev 1A
	Date: Wednesday, April 08, 2020 Sheet 100 of 106		



GPU Design	R-sense	VIN bead	SPCAP
N18P-G61/62	Stuff	Unstuff	2pcs

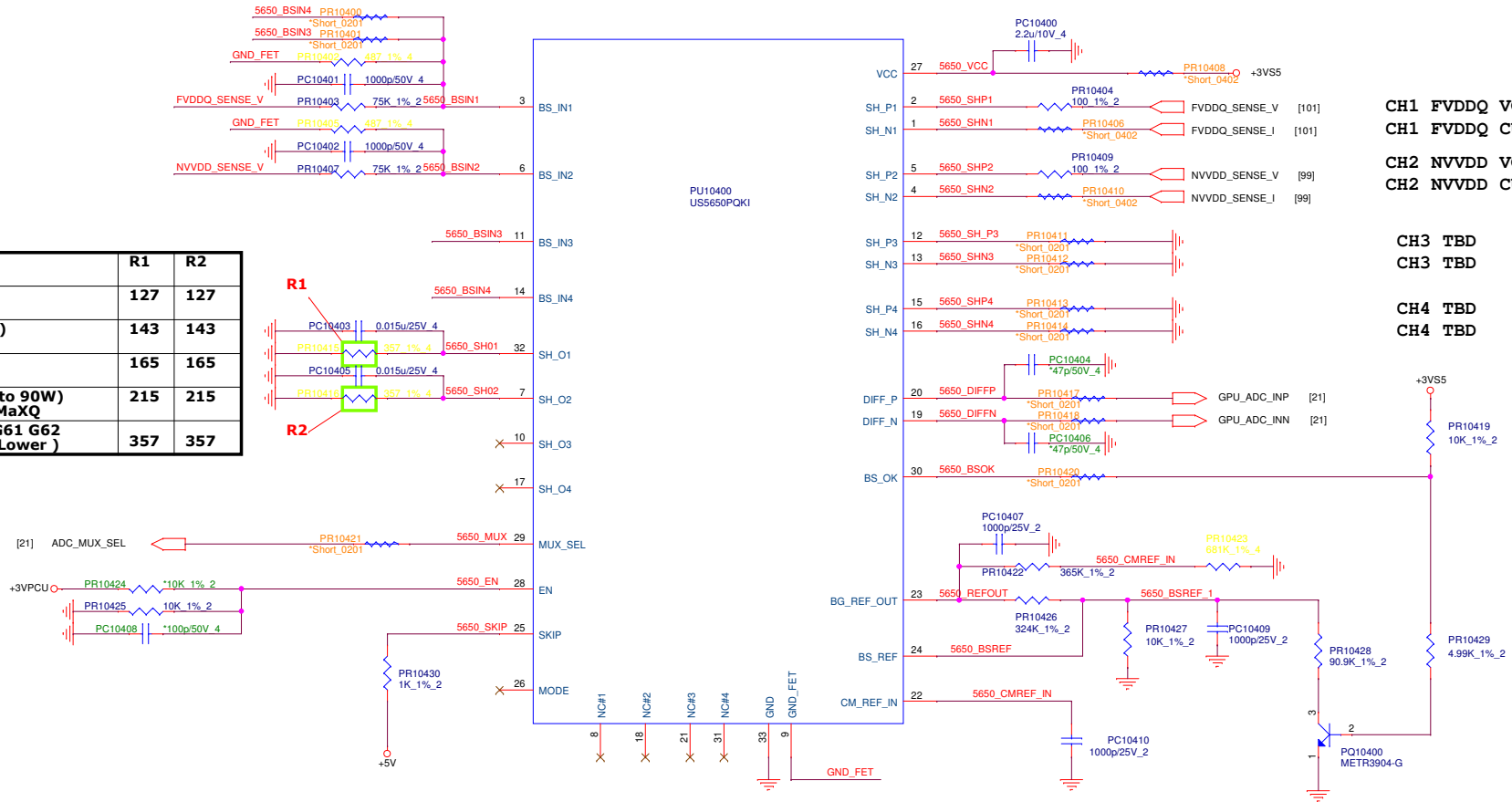
FBVDDQ_MEM	R1	R2	GPU Type
1.55V-1.35V	34.8K	53.6K	
1.5V_1.35V	30.9K	69.8K	N18P_N17P_GDDR5
1.25V_1.35V	21K	80.6K	N18E_GDDR6
1.2V_1.25V	16.9K	133K	N18P_GDDR6
Fix 1.35V	21K	Open	
Fix 1.5V	30.1K	Open	
MEM_VDD_CTRL	FBVDDQ_MEM		
1	1.2V		
0	1.25V		

	Ra	Re	Rf	OCp
N18P G61/62 1-Phase	Stuff	46.4K	86.6K	25A

Default setting

+3V [9,10,11,13,16,17,18,21,28,30,31,33,34,36,38,39,41,42,48,50,51,52,82,88,91,95,98,99,101,105]

UPI OVR Setting	R1	R2
N18E G3 (150W+)	127	127
N18E G2 (115W to 130W)	143	143
100W to 110W	165	165
N18E-G0,N18E-G1 (75W to 90W)	215	215
N18E-G2 MaxQ,N18E-G3 MaxQ		
N18P G0 N18P G0 MaxQ G61 G62	357	357
N18E G0 MaxQ (70W or Lower)		

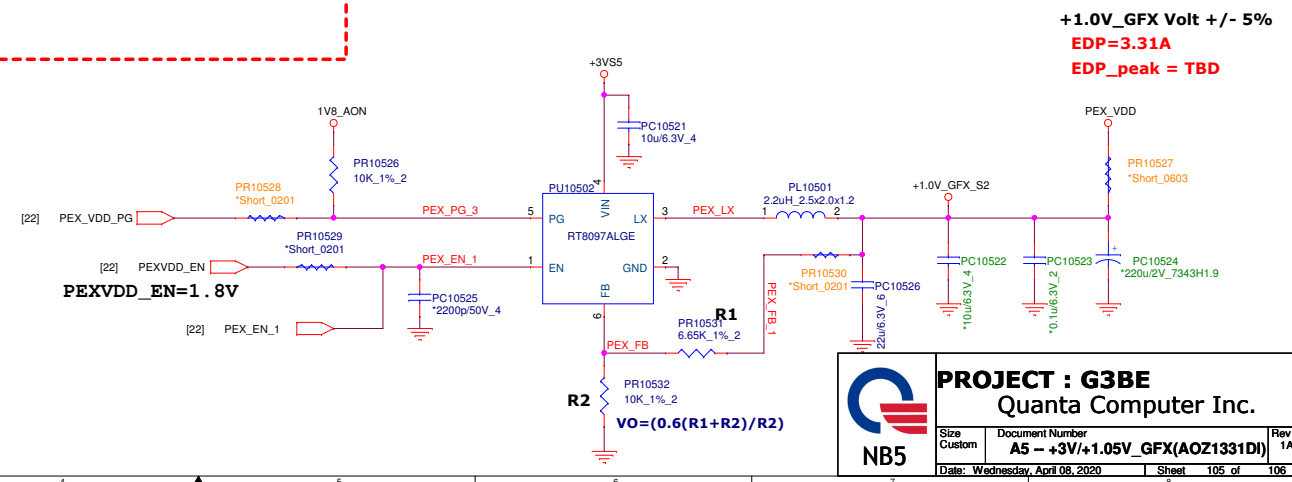
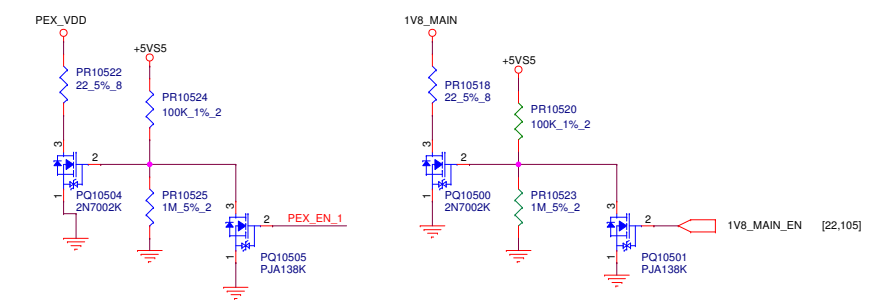
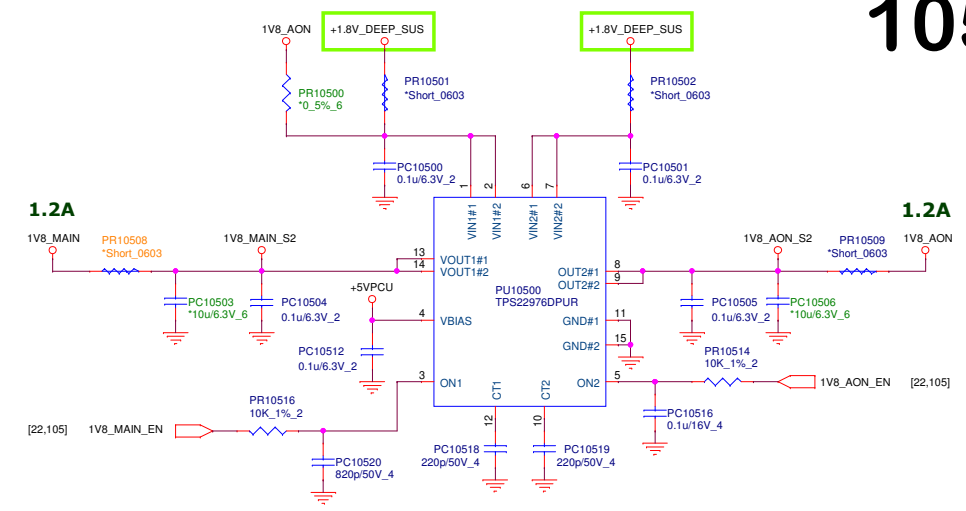


CH1 FVDDQ VOLTAGE
CH1 FVDDQ CURRENT

CH2 NVVDD VOLTAGE
CH2 NVVDD CURRENT

CH3 TBD
CH3 TBD

CH4 TBD
CH4 TBD



+BAT_RTC [10,12,14,34,82]
+3VPCU [10,32,34,35,42,43,46,48,51,82,86,88,104]

